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The study and characterisation of High-Flux CdZnTe using HEXITEC$_{MHz}$

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20/09/2023

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HEXITEC MHz

Funded by the: Centre for Instrumentation (CFI) run by Marcus French

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Agenda

1 HEXITEC vs HEXITEC$_{MHz}$

The next generation of HEXITEC systems

2 HEXITEC$_{MHz}$ Overview

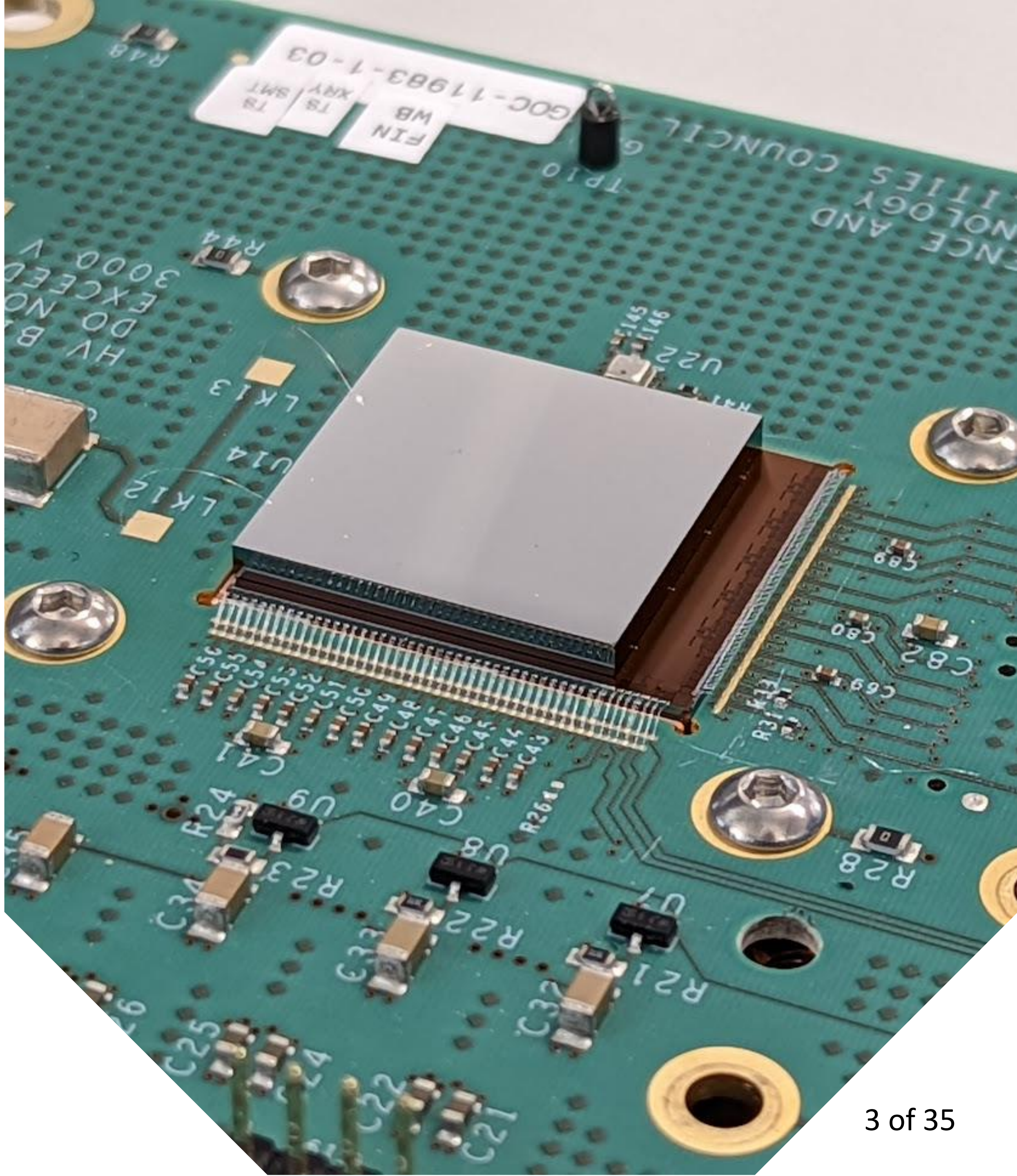
An introduction to our new HEXITEC$_{MHz}$ ASIC including its architecture and specification

3 HF-CZT Test Results

Characterisation of spectroscopic performance using a lab-based X-Ray source and Diamond Light Source synchrotron X-Rays

4 Next Steps

A look to the next 12 months



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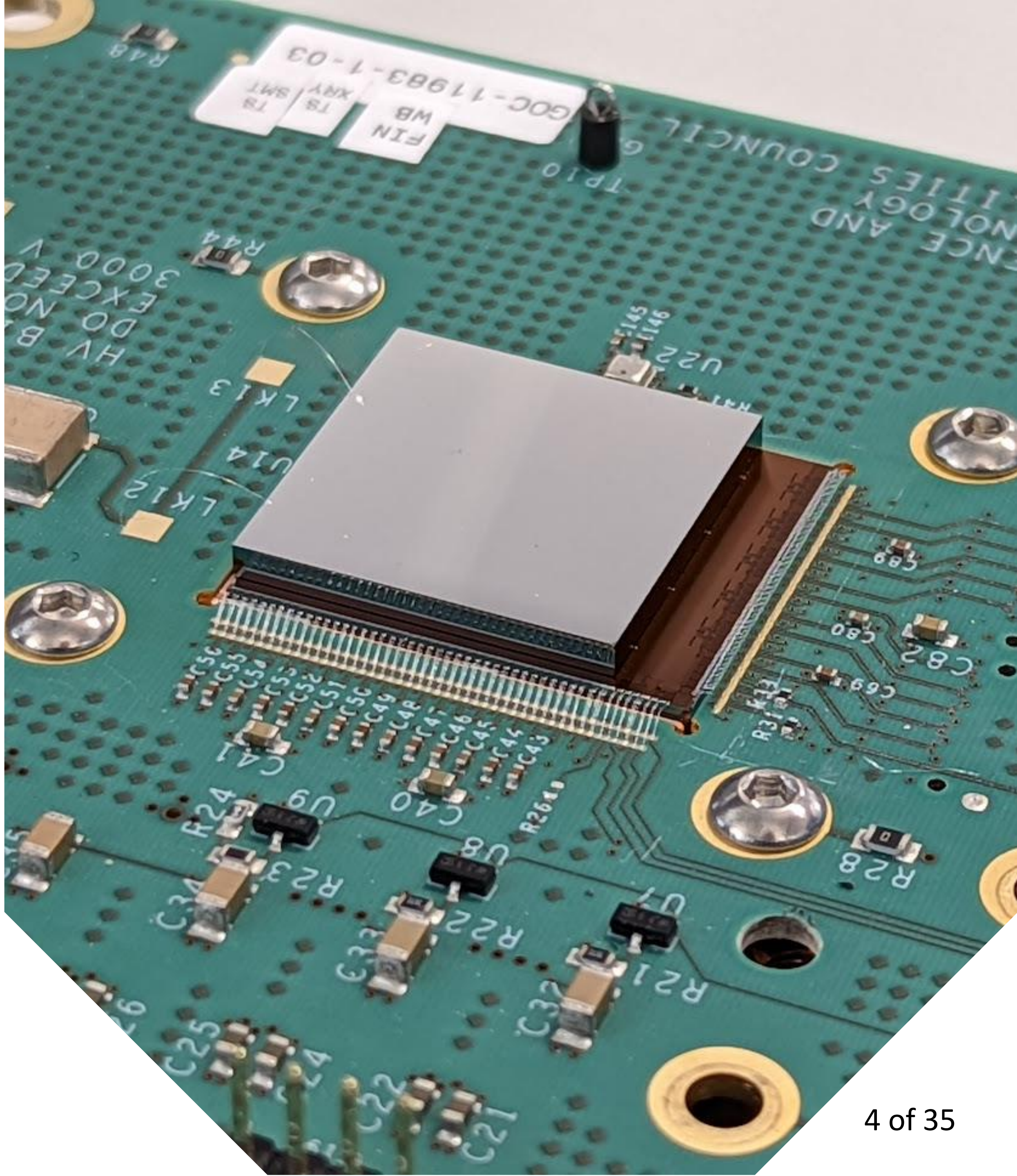
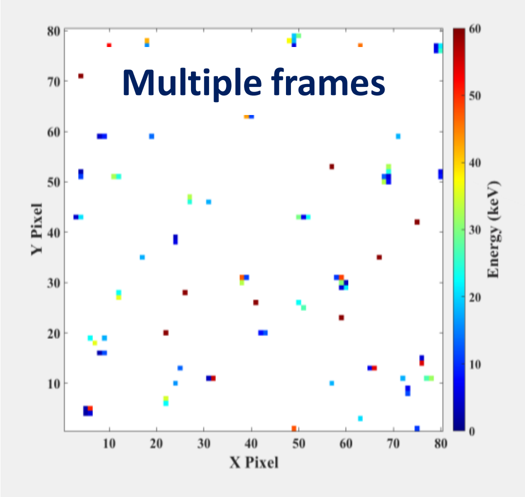
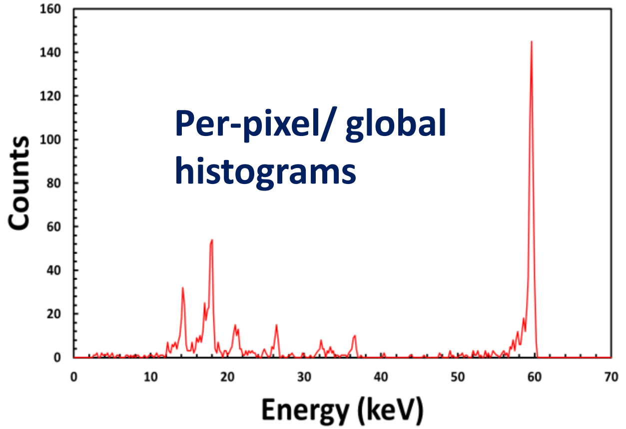


HEXITEC

HIGH ENERGY X-RAY IMAGING TECHNOLOGY

- **Fully spectroscopic X-Ray Imaging** with CdTe/ CdZnTe (CZT) detectors
- 80 × 80 pixel array on a 250 µm pitch
- **Analogue readout** via a rolling shutter to **4 ADCs in the DAQ**
- Maximum ~10 kHz data output (~100 MB s^{-1})
- AMS 0.35 µm - since 2010





HEXITEC specifications

Parameter	HEXITEC
Pixel Pitch (µm)	250
Array Size	80 × 80
Max Frame Rate (kHz)	~10
Max Spectroscopic Flux ($ph\ s^{-1}\ mm^{-2}$)	~10^4
Digitisation	Off-chip
Detector Type	Peak Track + Hold
Gain stages (keV in CZT)	200
	600
$FWHM_{@100keV}$ (keV in CZT)	<1 • HF-CZT: 0.79 keV @ 59.54 keV [1] • 300-µm thick p-type Si: 0.59 keV @ 59.54 keV [2]

[1] DOI: 10.3390/s20102747 [2] DOI: 10.1088/1748-0221/17/05/P05030

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HEXITEC
HIGH ENERGY X-RAY IMAGING TECHNOLOGY

- HEXITEC has been used across many applications including:

Compton X-Ray Imaging [3]

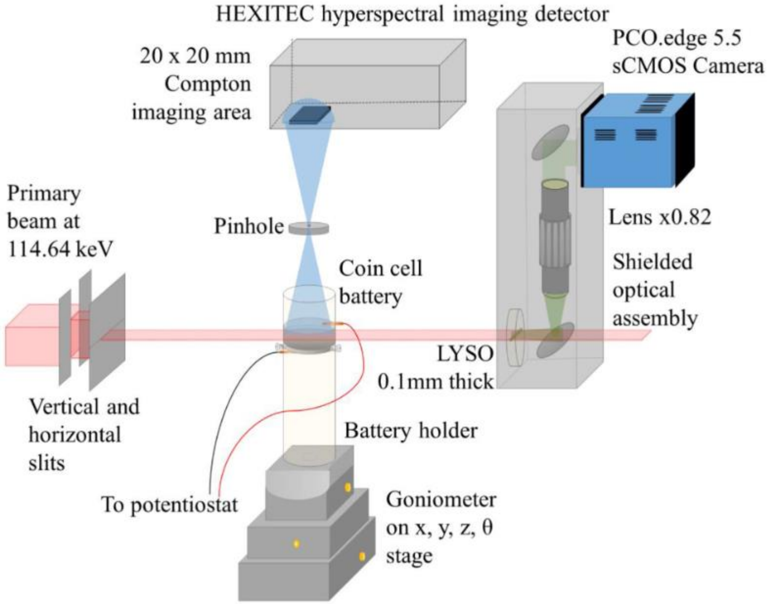

Figure 1. Schematic of the correlative X-Ray Compton scattering imaging (XCS-I) and X-Ray computed tomography (XCT) technique experimental set-up

X-Ray Fluorescence Imaging [4]

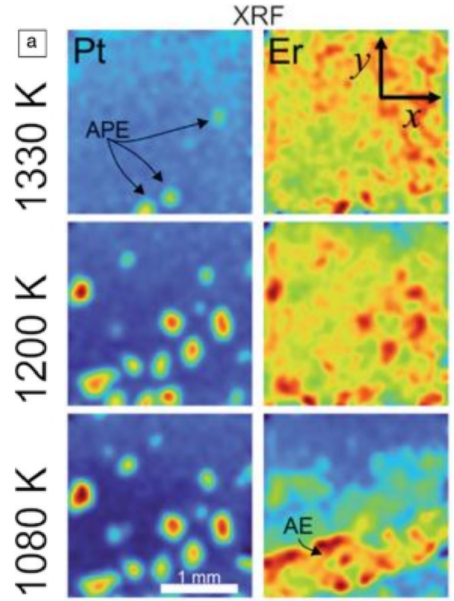

Figure 7. (a) Pt and Er XRF intensity maps as a function of temperature during the solidification of an Al-23Pt-20Er alloy at 0.1 Ks^{-1}.

Hyperspectral X-Ray Tomography [5]

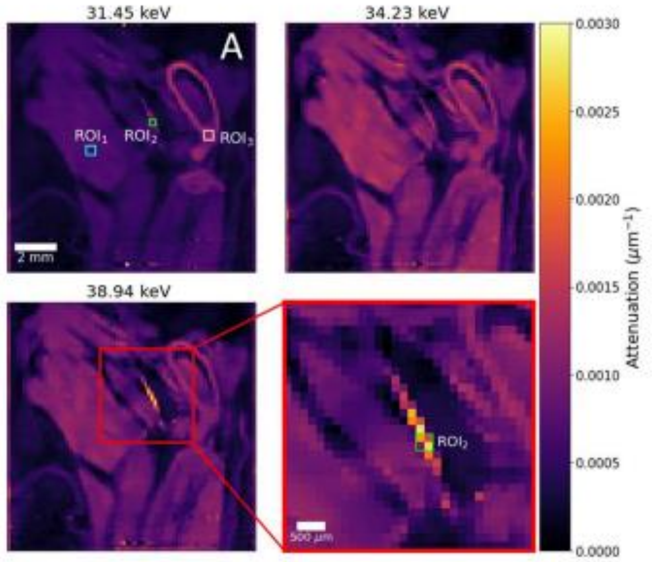

Figure 2. Voxel spectra analysis for double-stained hindlimb specimen. (A) Single image slice in the sagittal plane across three monochromatic energy channels, following iterative reconstruction. A set of three regions-of-interest (ROIs) are highlighted for voxel spectra analysis.

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[3] DOI: 10.1016/j.mtener.2022.101224 **[4]** DOI: 10.1557/mrs.2020.270 **[5]** DOI: 10.1038/s41598-022-23592-0

HEXITEC
HIGH ENERGY X-RAY IMAGING TECHNOLOGY

BUT …

- **HEXITEC is frame-rate and therefore flux limited**
  - Charge-sharing corrections require <10 % frame occupancy
  - This limits spectroscopic imaging @10 kHz to a **max X-Ray flux of ~10^4 ph s^{-1} mm^{-2}**

→ There is a need for a continuous spectroscopic X-Ray detector that operates at faster frame rates

- **Faster (MHz) imaging requires**:
  - In-pixel digitisation
  - High-speed serialisers
  - Dedicated FPGA processing

- These **requirements apply to a large number of STFC's upcoming detector development projects**
  - E.g. DynamiX, C100

UKRI Science and Technology Facilities Council

HEXITEC$_{MHz}$

A new fully spectroscopic X-Ray imaging detector:

- 80 × 80 pixels on a 250 μm pitch
- New front-end design – now an **integrating** detector
- **On-chip 12-bit digitisation** (no external ADCs)
    - Data outputted via **20 × 4.1 Gbps serialisers**
- **1 MHz continuous frame rate**
    - Spectroscopic X-Ray fluxes of **>10^6 ph s^{-1} mm^{-2}**

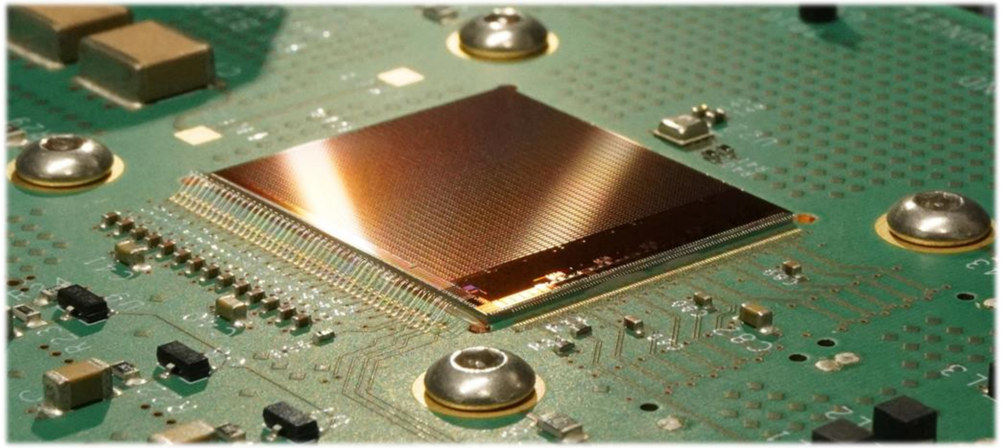

Photo of ASIC

Comparison of HEXITEC and HEXITEC$_{MHz}$ specifications

Parameter	HEXITEC	HEXITEC$_{MHz}$
Pixel Pitch (μm)	250	250
Array Size	80 × 80	80 × 80
Max Frame Rate (kHz)	~10	**1000**
Max Spectroscopic Flux (ph s^{-1} mm^{-2})	~10^4	**>10^6**
Digitisation	Off-chip	**On-chip**
Detector Type	Track + Hold	**Integrating**
Gain Stages (keV in CZT)	200	100
	600	200
		300
FWHM@100keV (keV in CZT)	<1	<1
Power Consumption (W)	1.5	15

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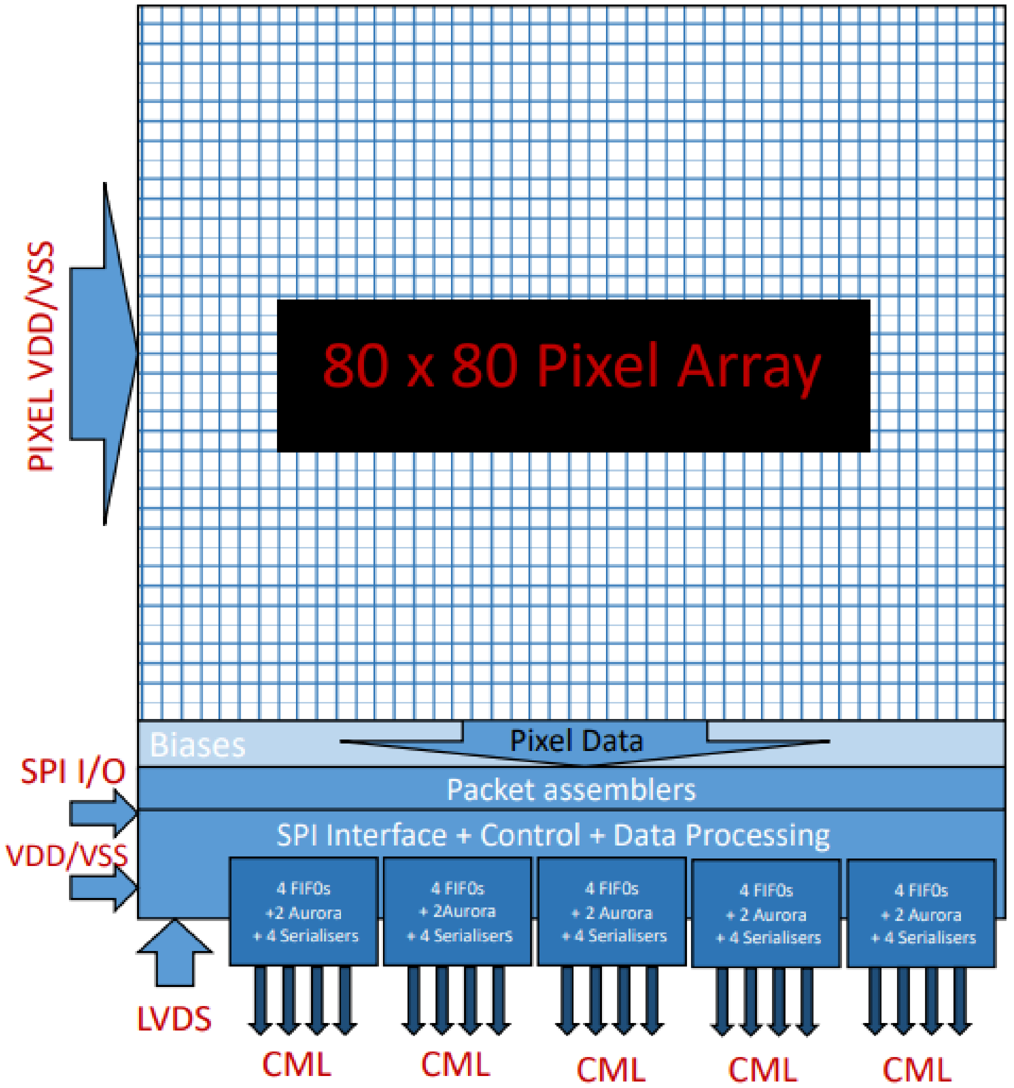
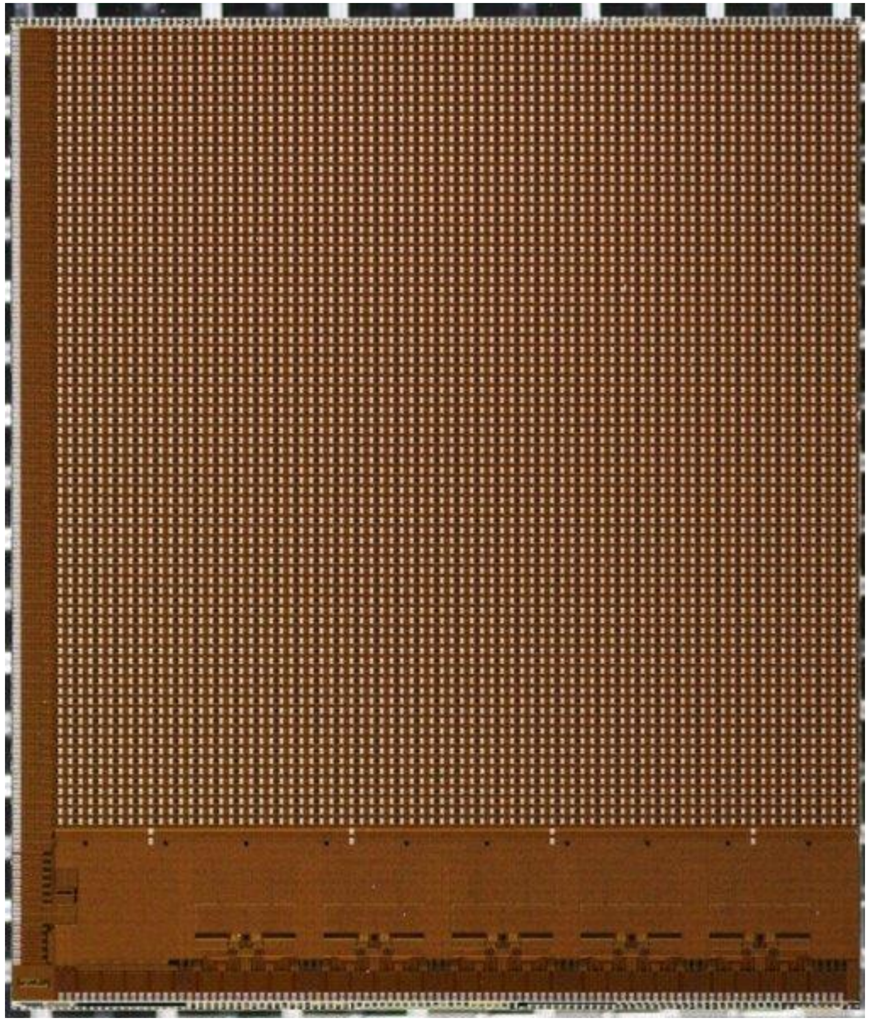
HEXITEC$_{MHz}$



ASIC block diagram



HEXITEC$_{MHz}$ ASIC

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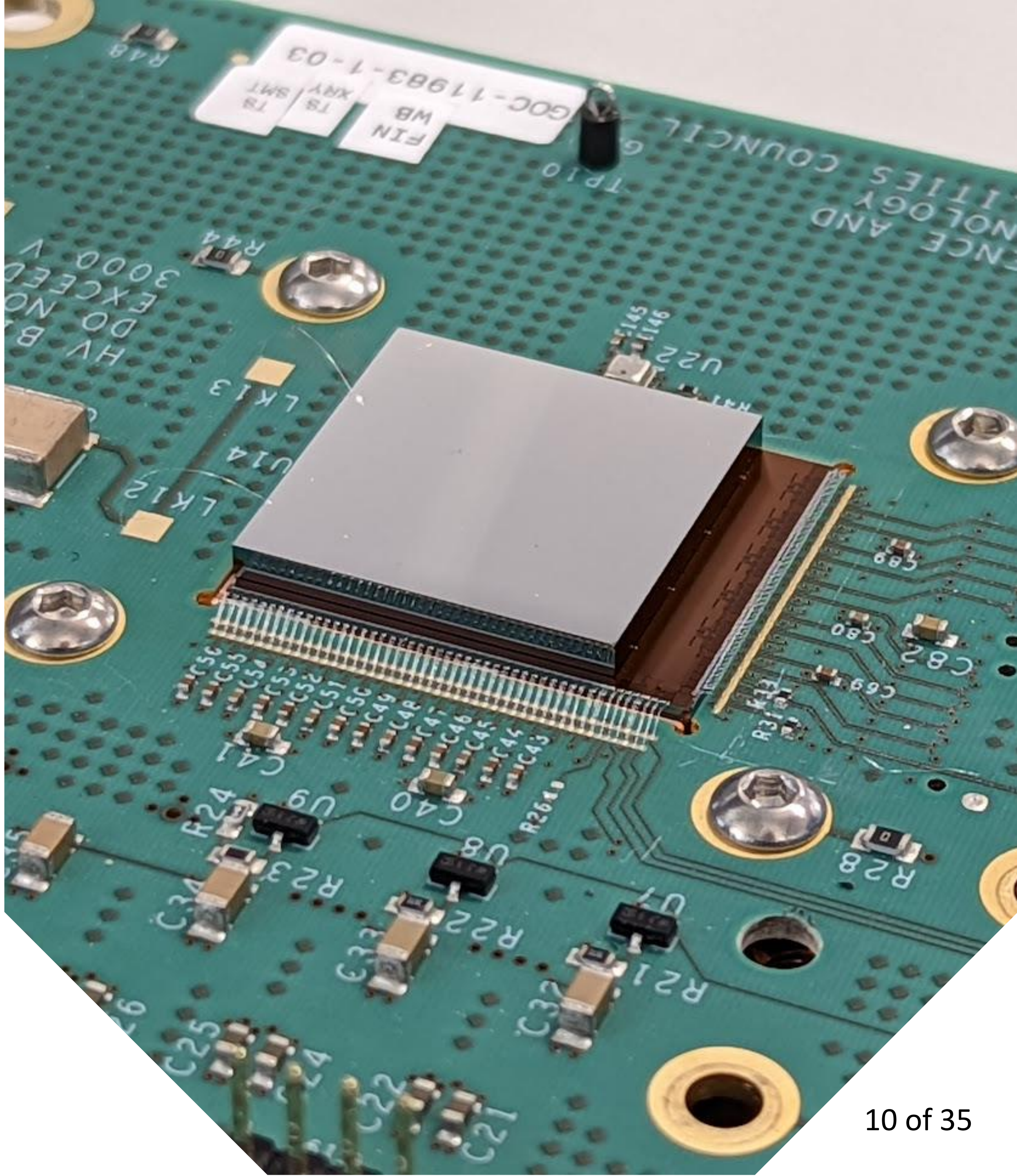
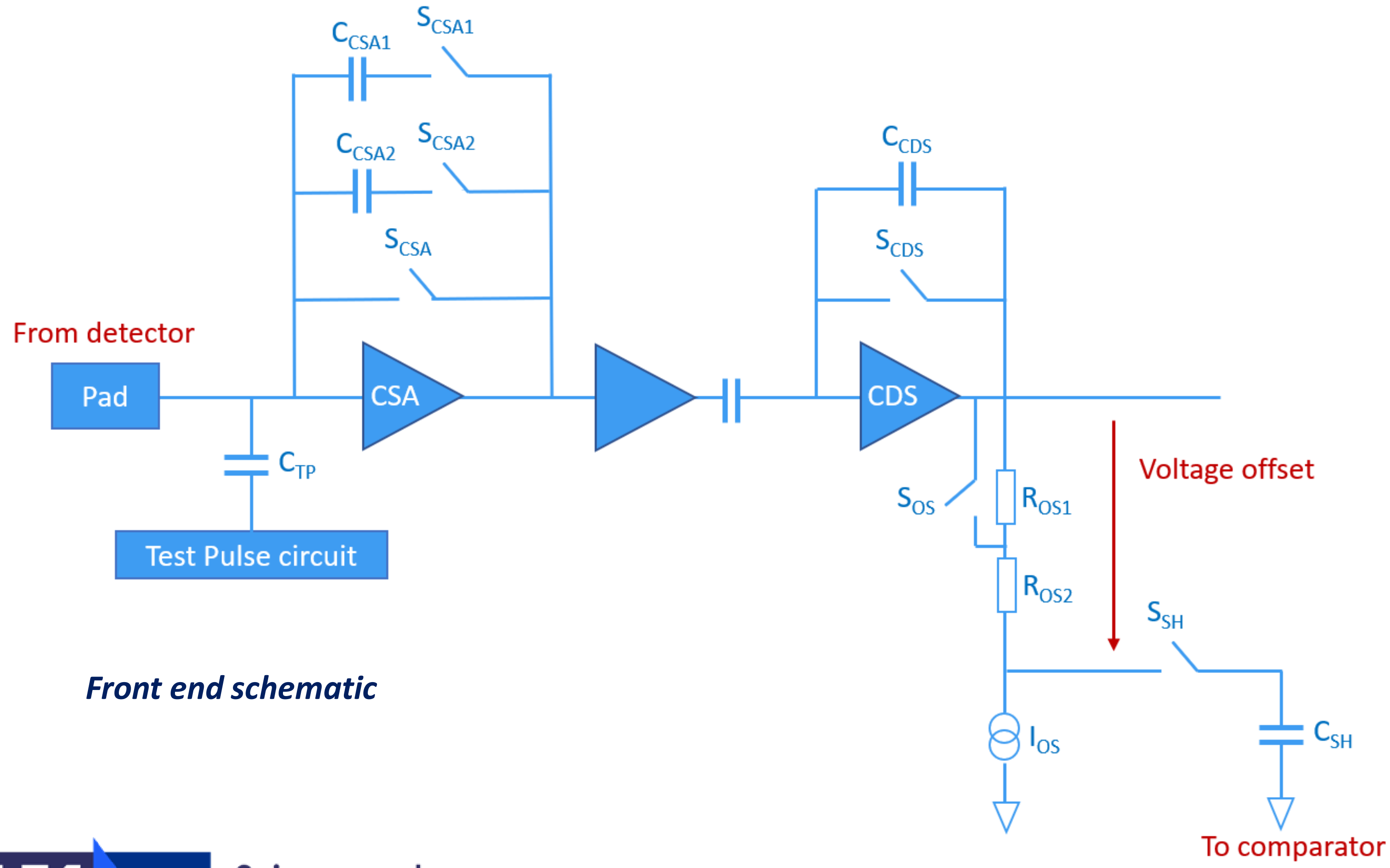


HEXITEC$_{MHz}$ - Integrating Front End



Front end schematic

Properties:

- CSA + CDS amplifier
- 3 static dynamic ranges
- $t_{10\text{-}90}$ = 50 ns
- t_{reset} ≈ 90 ns
- ENC < 70 e^-

Gain	C_{CSA1} (7 fF)	C_{CSA2} (14 fF)	Dynamic Range (keV in CZT)
Low	✓	×	~300
Medium	×	✓	~200
High	✓	✓	~100

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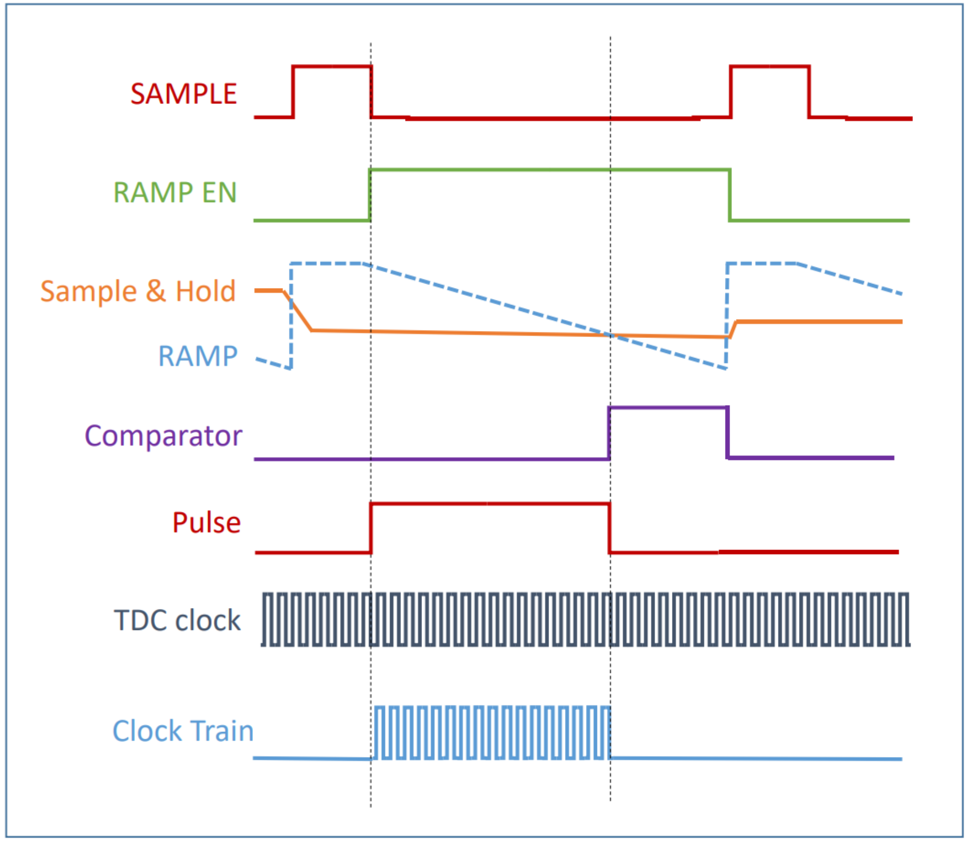
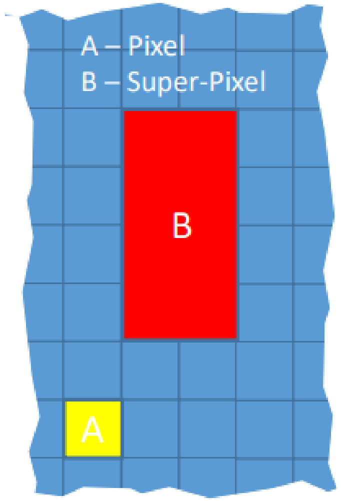
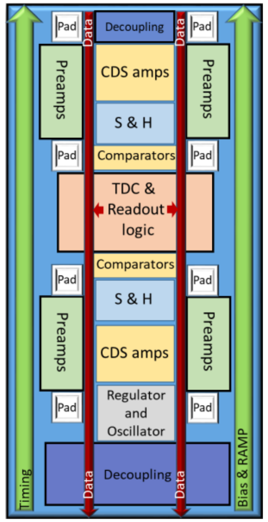
HEXITEC$_{MHz}$ - In-Pixel TDC



TDC signal timing

- **12-bit** digitisation
  - **The Sample & Hold signal is compared with a ramp with a programmable slew**
- The ASIC comprises **800 super-pixels of 2 × 4 pixels**
  - These contain **one TDC block and shared readout logic**





Super-pixel schematics

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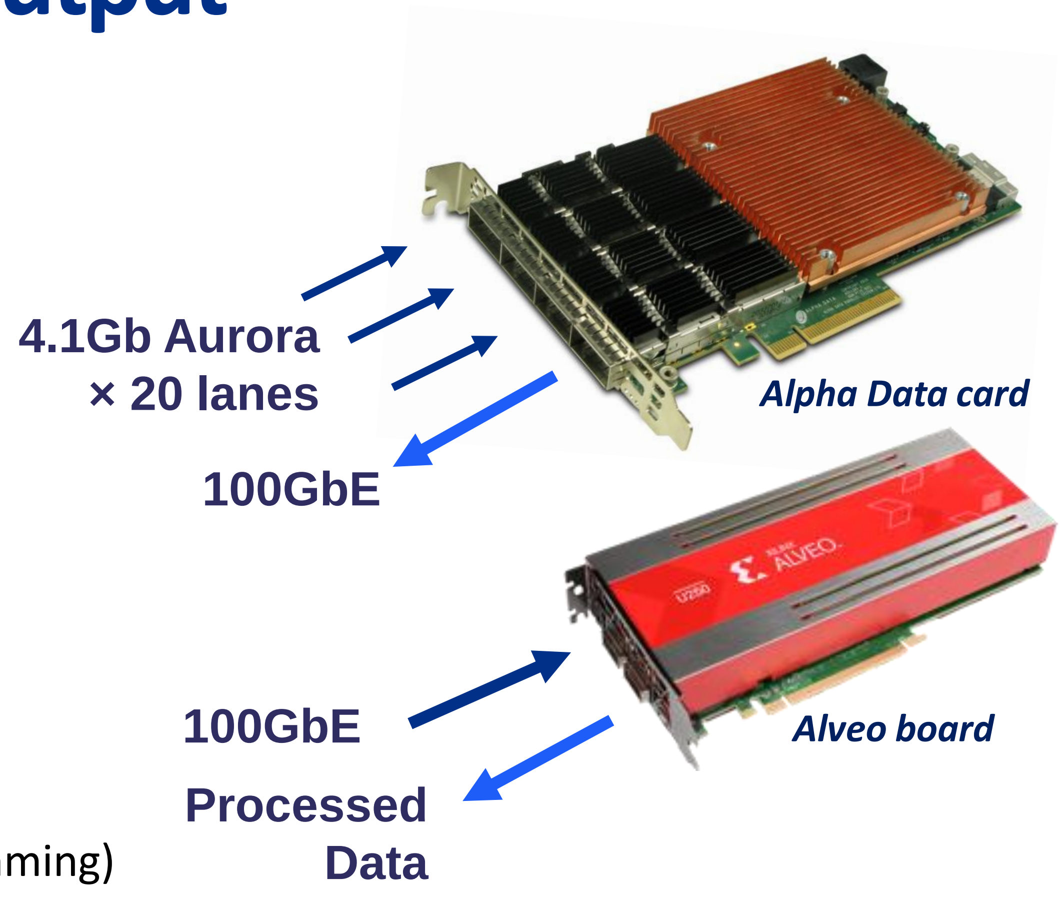
HEXITEC$_{MHz}$ - Data Output

- 80 × 80 array is divided into **divisions of 4 columns**
  - Each division has **packet-assembler** and dedicated **serialiser**
  - Packets constructed using **Xilinx's Aurora 64B/66B protocol**
  - Serialisers operate at **4.1 Gb s^{-1} (total data rate ≈ 10 GBs^{-1})**



What to do with all this data?

- Two receiving data planes:
  - **First-stage FPGA – Alpha Data card**
    - Recovers and reorders the received optical data
  - **Second-stage FPGA – Xilinx Alveo U50 board**
    - Data corrections (darks, energy calibration)
    - Data reduction (charge-sharing discrimination, histogramming)

- Then received by **ODIN Data, a scalable data-processing and acquisition network**

HEXITEC$_{MHz}$ - Data Output

- 80×80 array is di
  - Each divisio
  - Packets co
  - Serialisers c

What to do with a

- Two receiving da
  - **First-stage**
    - Recove
  - **Second-sta**
    - Data c
    - Data red

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Journal of Instrumentation

PAPER • OPEN ACCESS

Spectroscopic X-ray imaging at MHz frame rates — the HEXITEC$_{MHz}$ ASIC

L. Jones[2,1], S. Bell[1], B. Cline[1], T. Gardiner[1], M. Hart[1], M. Prydderch[1], P. Seller[1], M. Veale[1] and M. Wilson[1]

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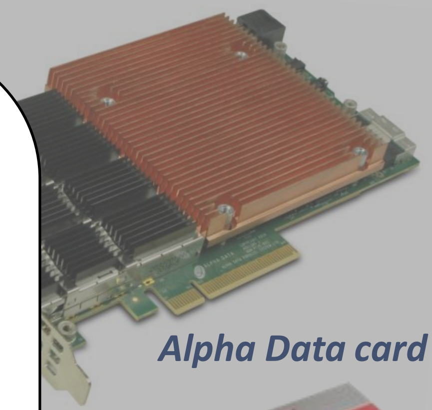

Alpha Data card

Alveo board

- Then received by **ODIN Data, a scalable data-processing and acquisition network**

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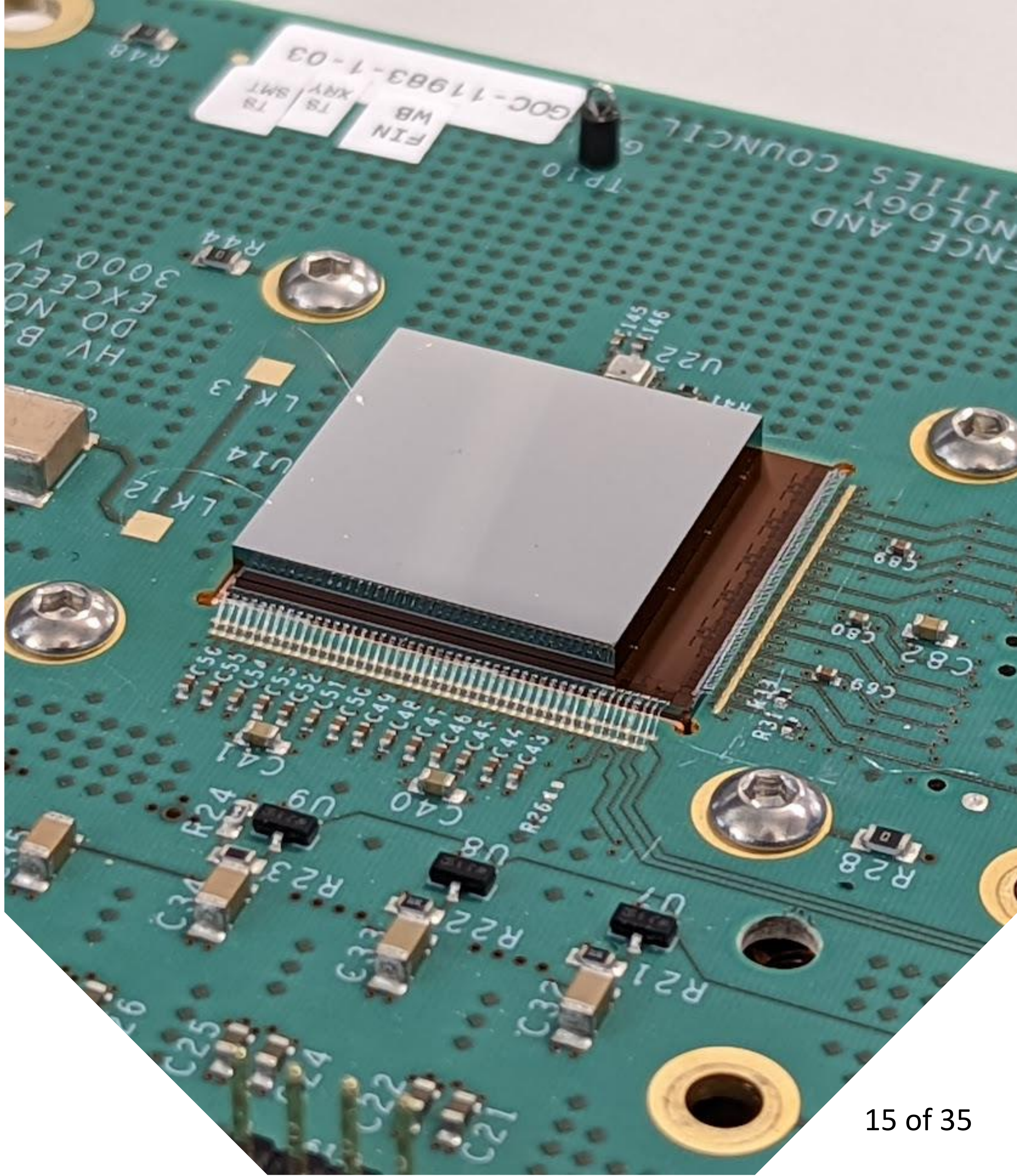
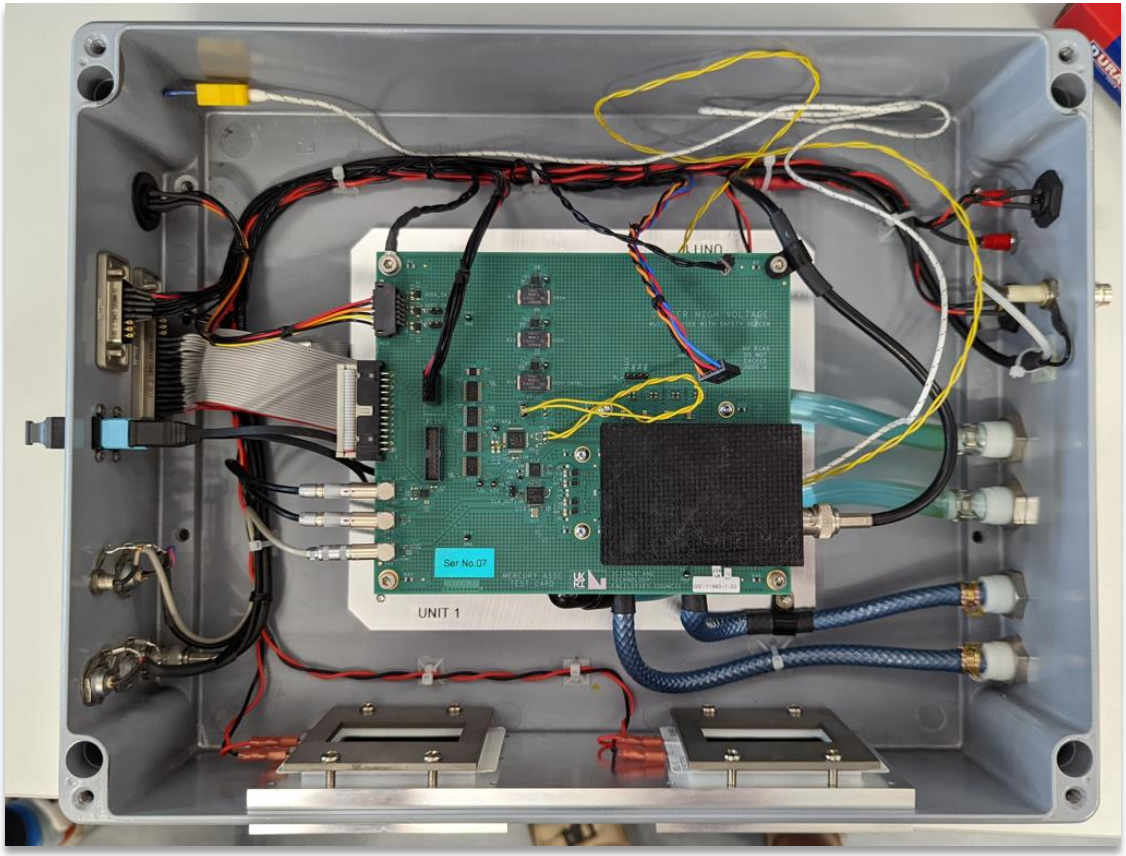
Agenda



Current Status

50 cm

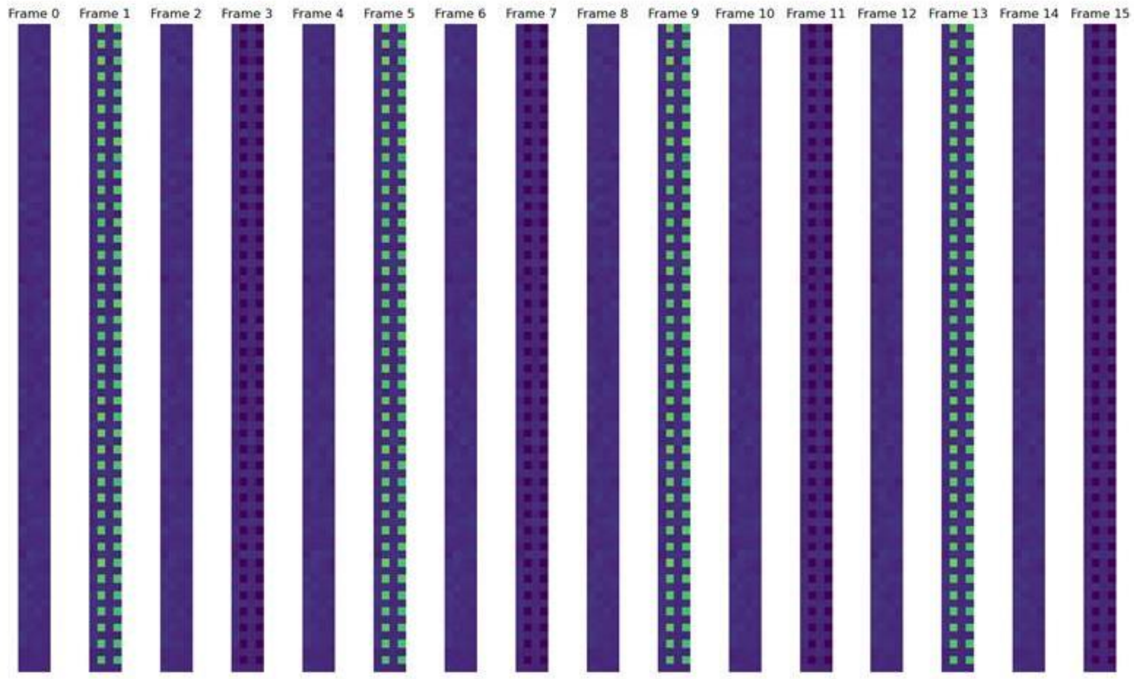


30 cm

HEXITEC$_{MHz}$ test enclosure

- ASIC is fully functioning
- Using **test enclosure**
- FPGA firmware in development – at present, **1 channel (4 × 80 pixels) over fast data**

15 µs



1 µs

Fast data output

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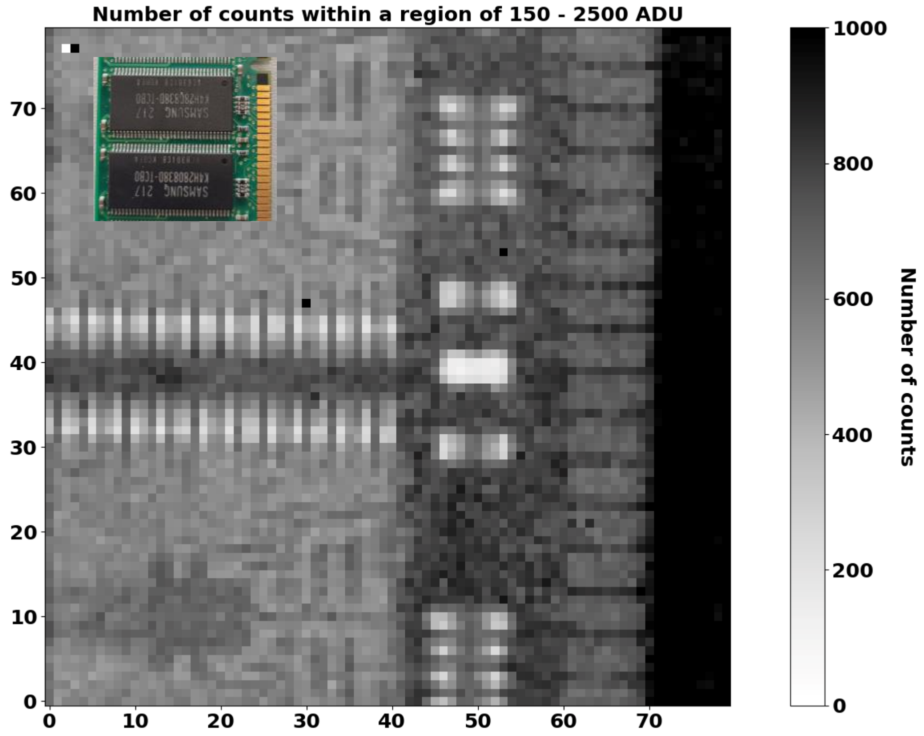
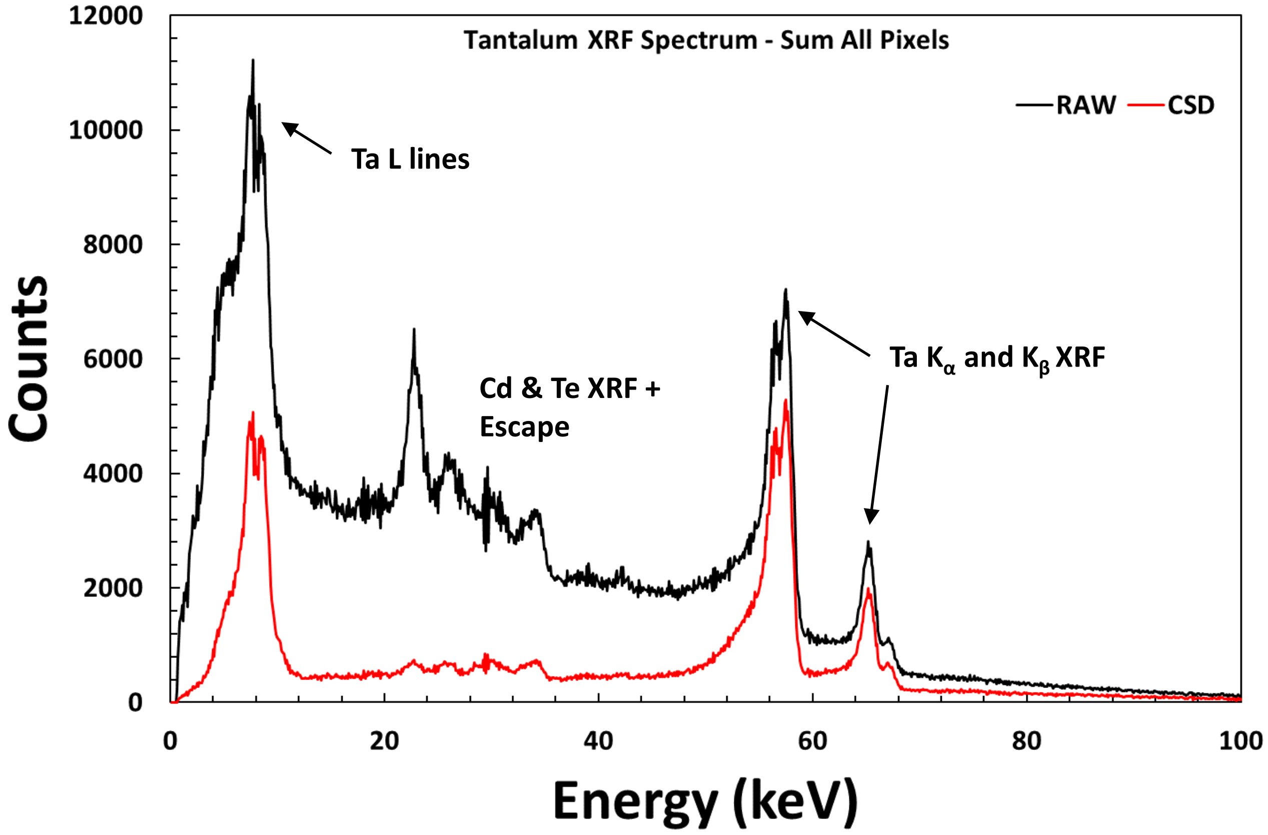
Testing – Initial X-Ray Tests



X-Ray transmission measurements of a DDR Ram Card using a HEXITEC_{MHz} HF-CZT sensor



X-Ray Fluorescence (XRF) measurements of Ta foil using a HEXITEC_{MHz} HF-CZT sensor in medium-gain mode

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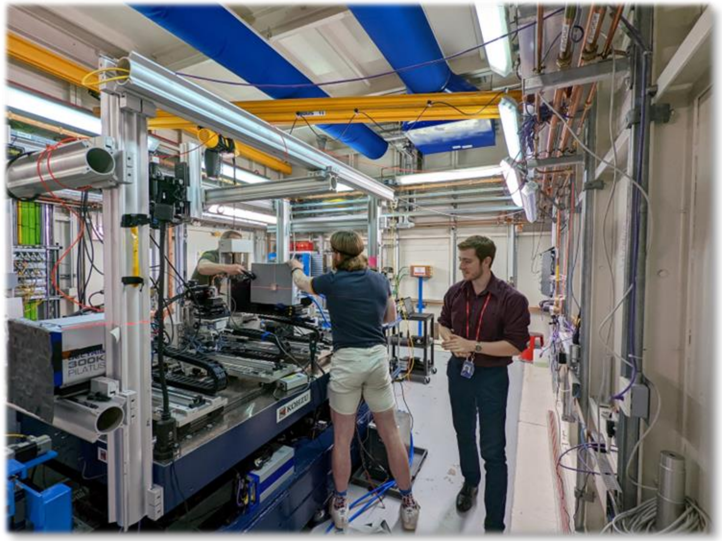
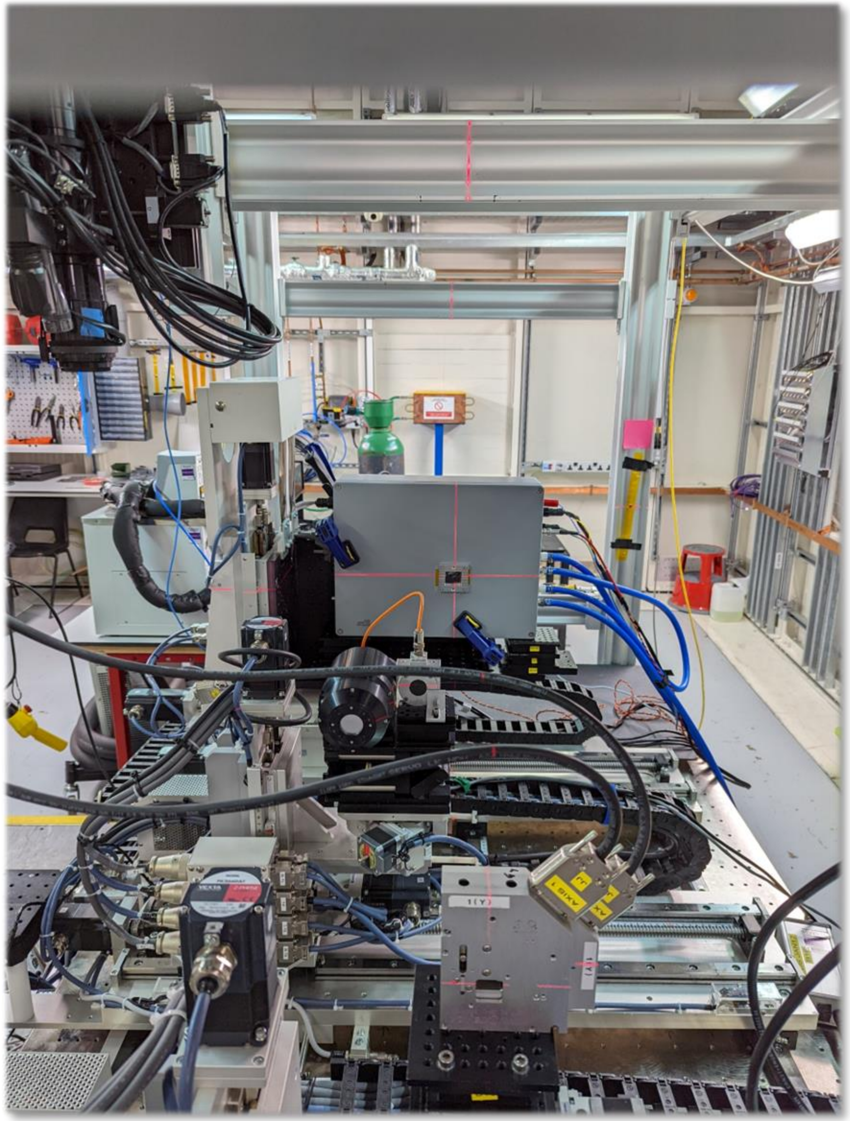
Experimentation at diamond

- **B16 Beamline: August and December 2022**
  - Monochromatic X-Rays: 10 – 20 keV
  - Photon fluxes: **10^5 – 10^8 ph s^{-1} mm^{-2}**
  - 1 MHz data stream on one fast-data channel
  - Tested **HF-CZT (2 mm), p-type Si (300 µm), GaAs (500 µm)** devices

- Beamline scientists: Vishal Dhamgaye, Oliver Fox, Kawal Sawhney





B16 setup photos

Experimentation at diamond

- **B16 Bea**
  - M
  - Ph
  - 1 M
  - Te
- Beamlin

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Journal of Instrumentation

PAPER • OPEN ACCESS

Preliminary characterisation of the $\text{HEXITEC}_{\text{MHz}}$ spectroscopic X-ray imaging detector

M.C. Veale[1], S. Bell[1], B.D. Cline[1], I. Church[1], S. Cross[1], C. Day[1], M. French[1], T. Gardiner[1], N. Ghorbanian[1], M.D. Hart[1] + Show full author list

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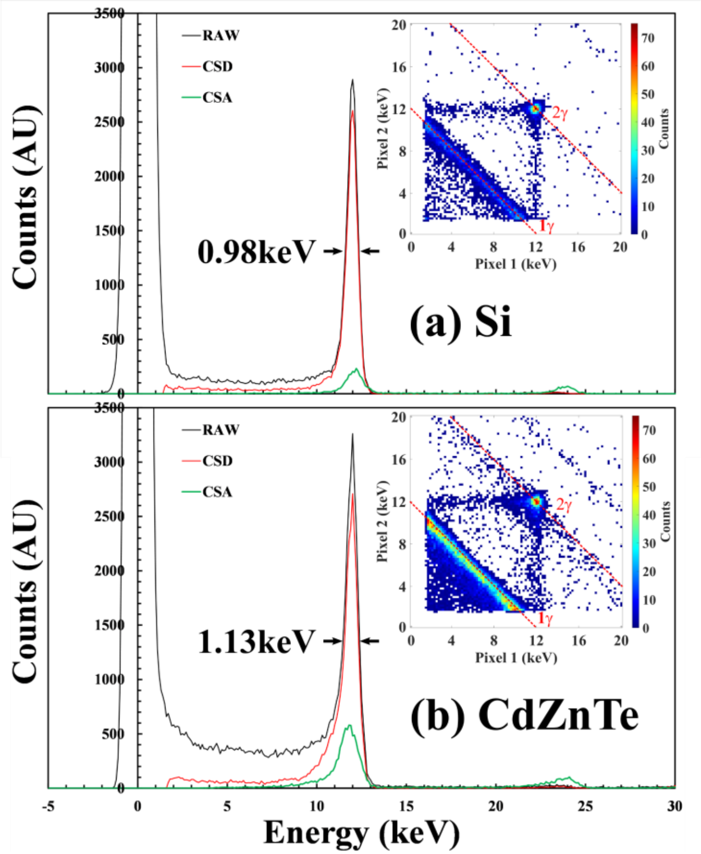
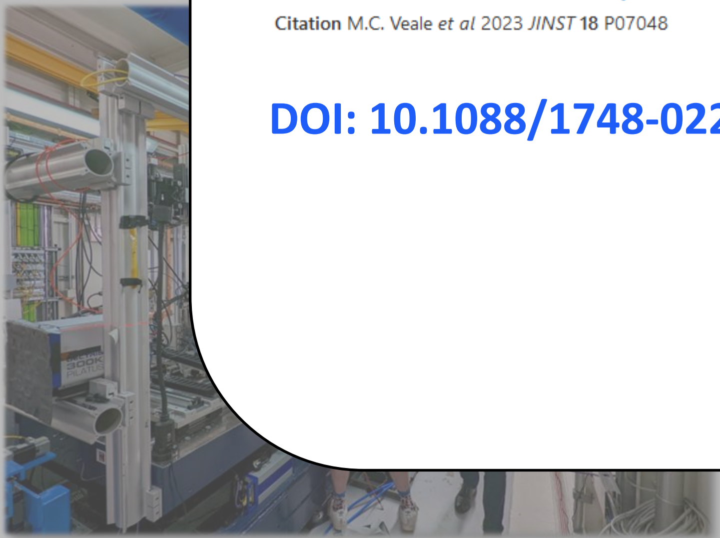
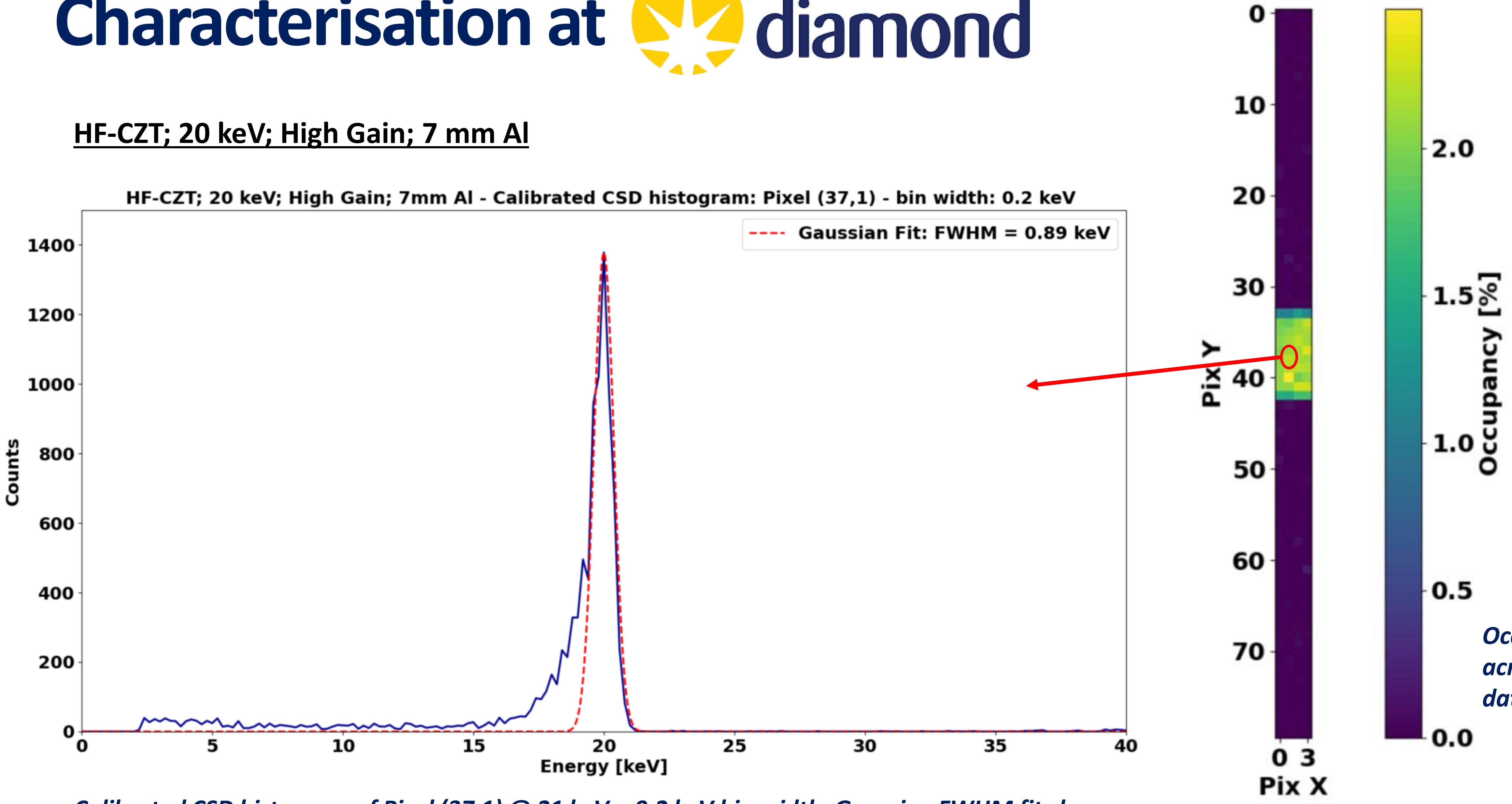




B16 setup photos

Characterisation at diamond

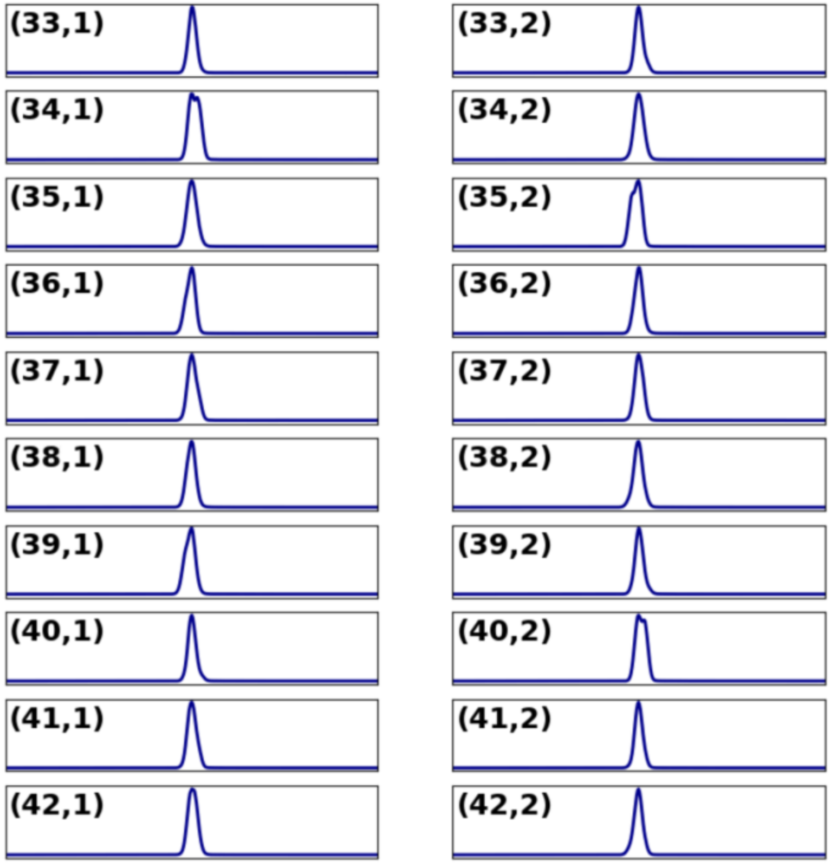
<u>HF-CZT; 20 keV; High Gain; 7 mm Al</u>



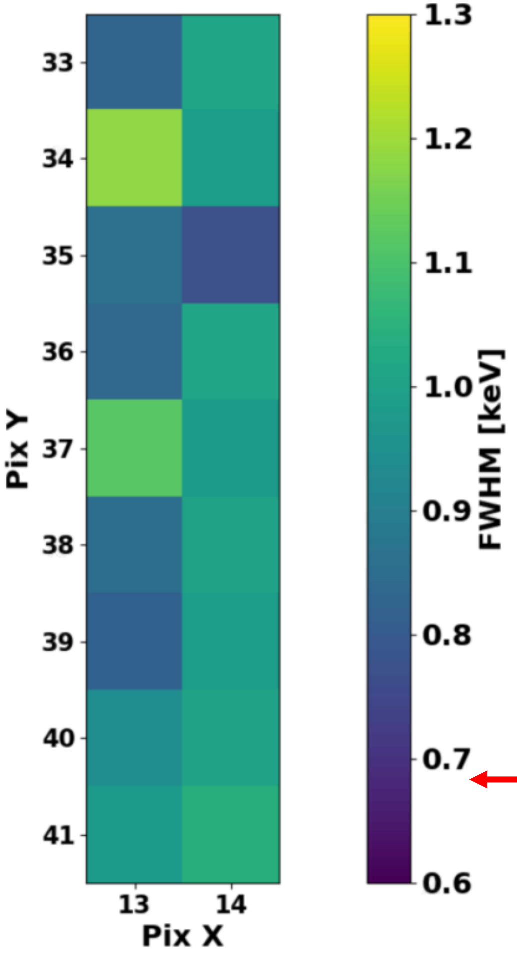
Occupancy across fast-data channel

Calibrated CSD histogram of Pixel (37,1) @ 21 keV – 0.2 keV bin width. Gaussian FWHM fit shown

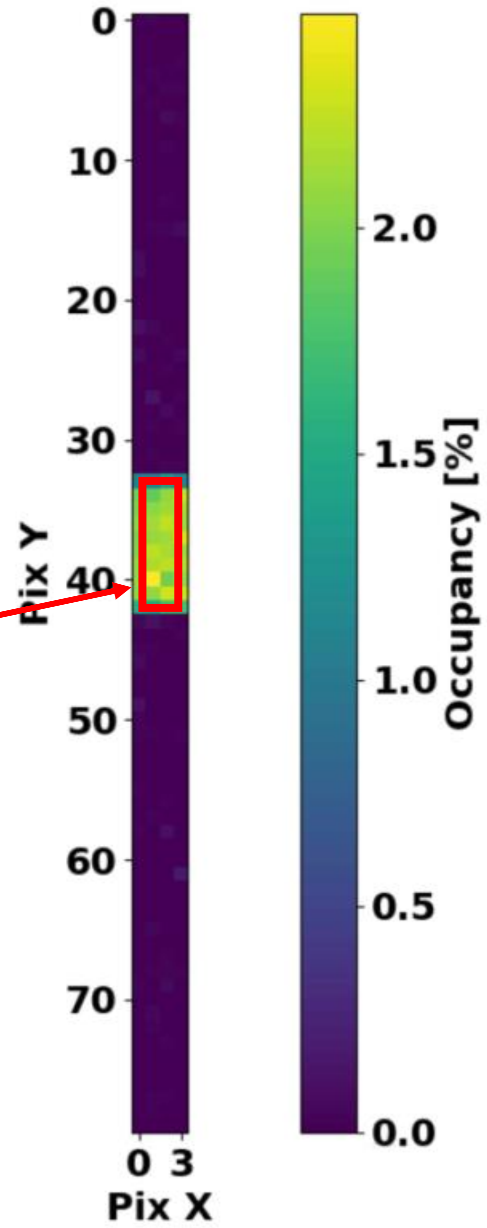
Characterisation at diamond



Calibrated CSD histograms in beam area



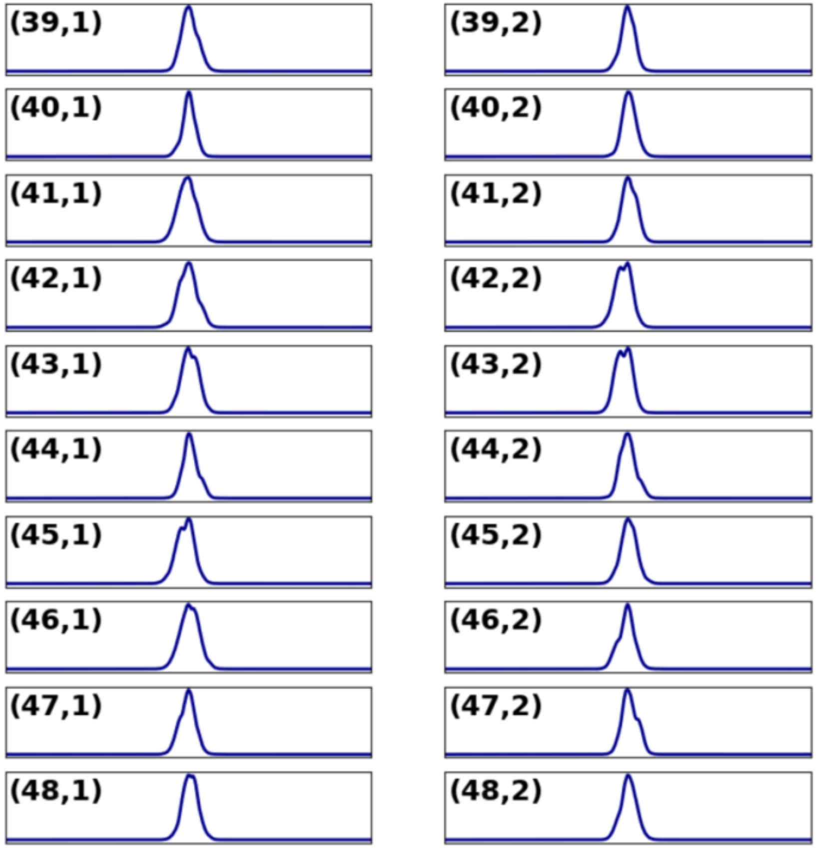
Single photon FWHM in beam area



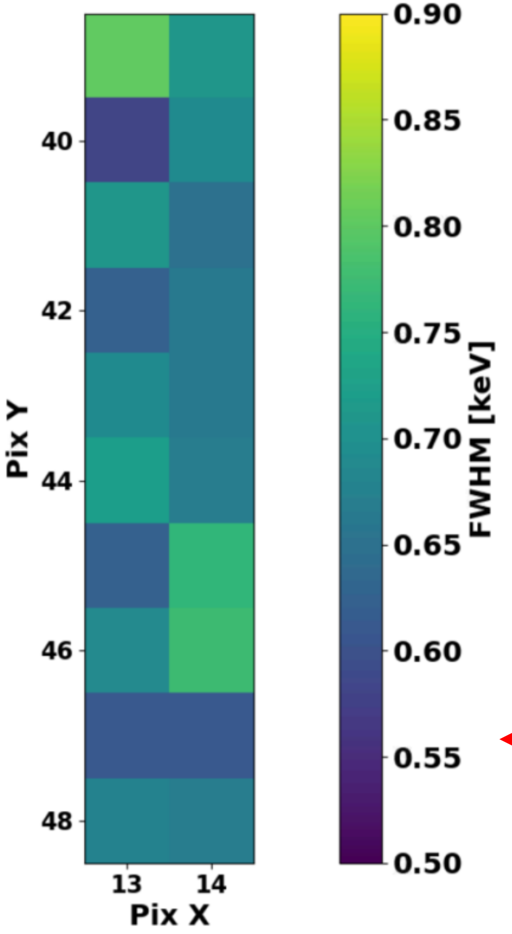
Occupancy across fast-data channel

Characterisation at diamond

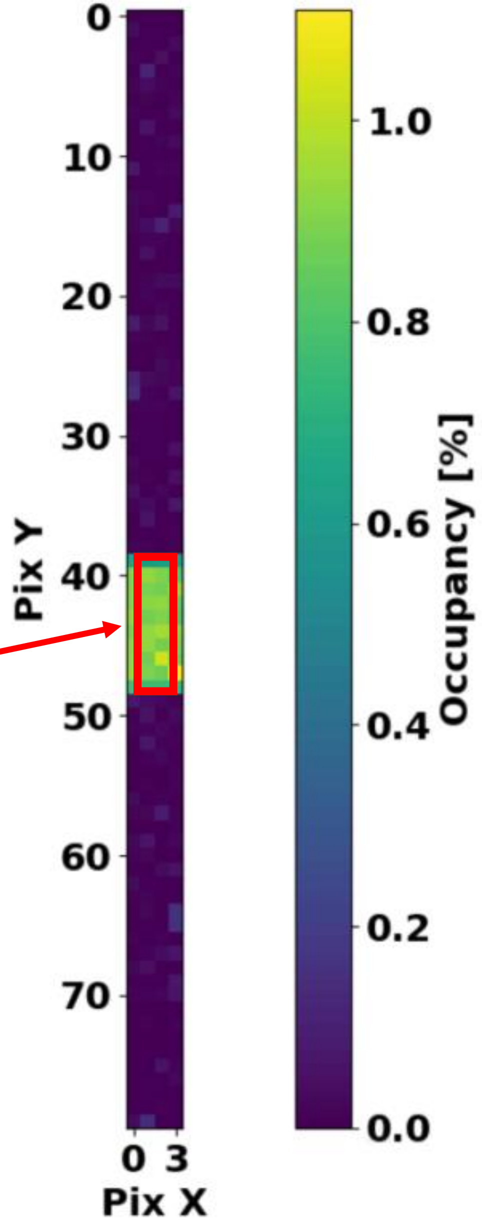
p-type Si; 15 keV; High Gain; 3 mm Al



Calibrated CSD histograms in beam area

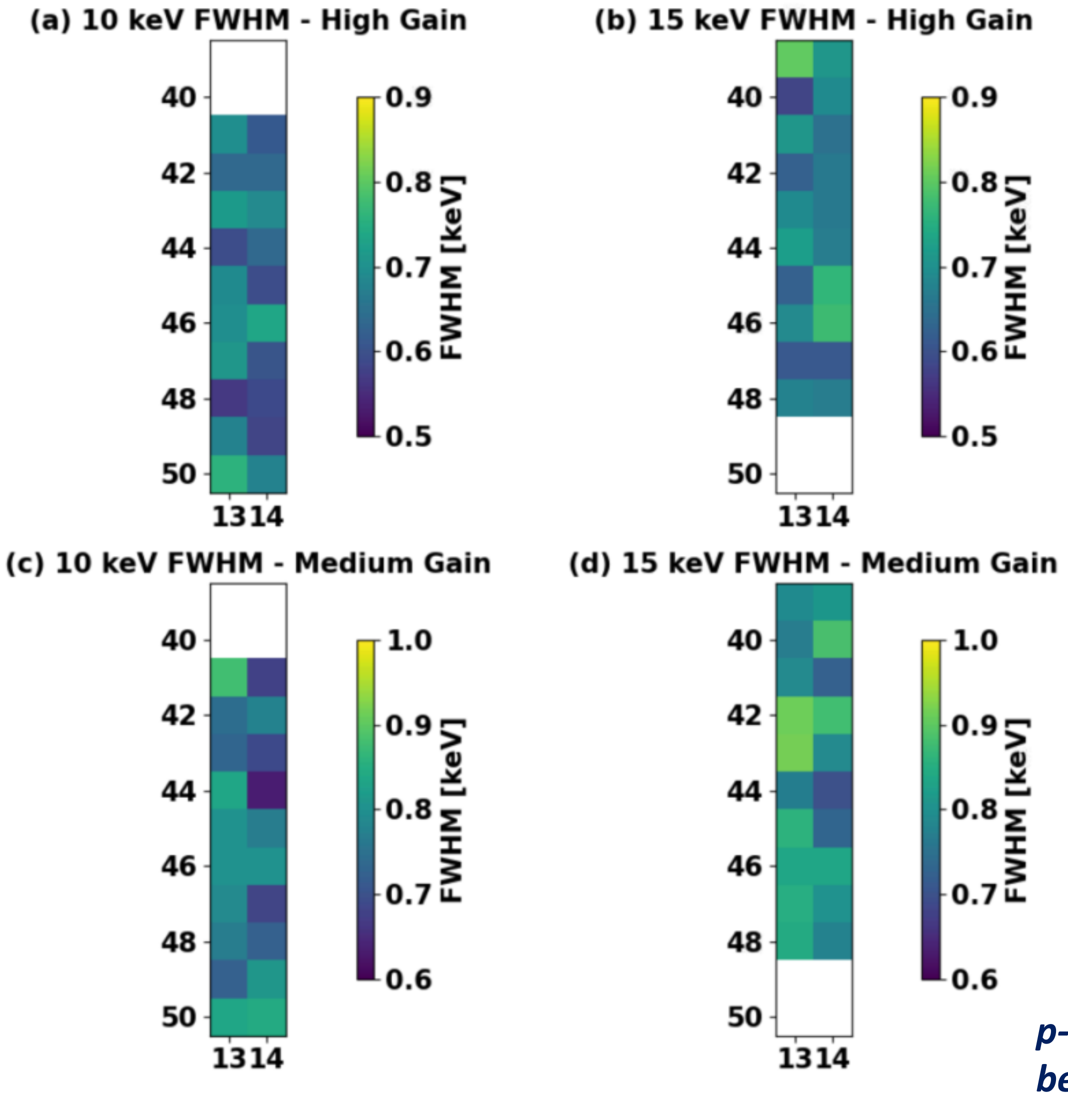


Single photon FWHM in beam area



Occupancy across fast-data channel

Characterisation at diamond



p-type Si FWHM in beam area

HF-CZT

Peak Energy [keV]	HG FWHM [keV]	MG FWHM [keV]	LG FWHM [keV]
20	0.85 ± 0.10	0.92 ± 0.11	1.13 ± 0.12

p-type Si

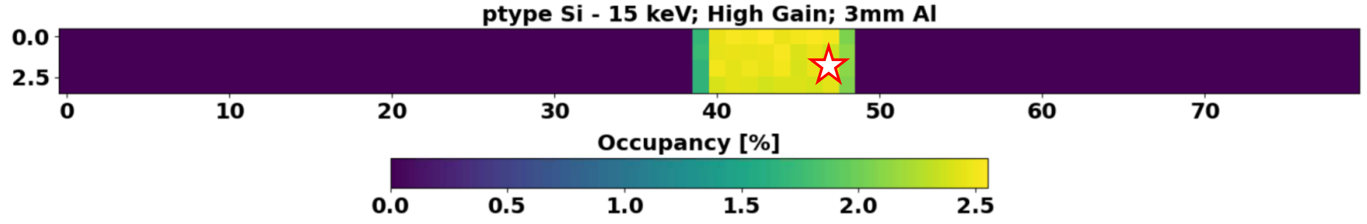
Peak Energy [keV]	HG FWHM [keV]	MG FWHM [keV]
10	0.66 ± 0.06	0.77 ± 0.06
15	0.68 ± 0.06	0.81 ± 0.06

Electron-hole pair generation energies

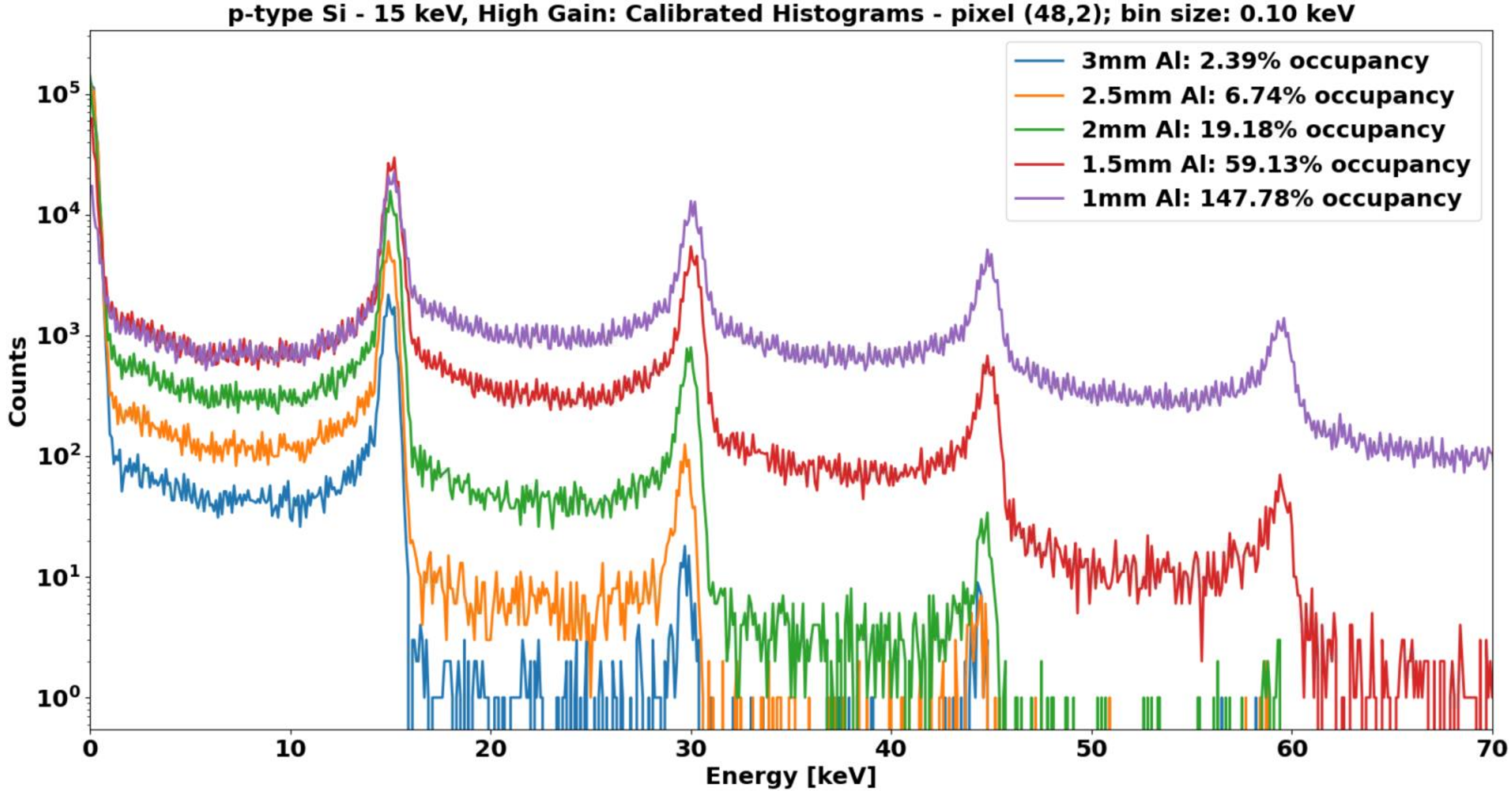
- CZT – 4.6 eV $(e\text{-}h\ pair)^{-1}$
- Si – 3.6 eV $(e\text{-}h\ pair)^{-1}$

Integrating Measurements at diamond

P-type Si; 15 keV; High Gain; 3 mm Al – 0 mm Al



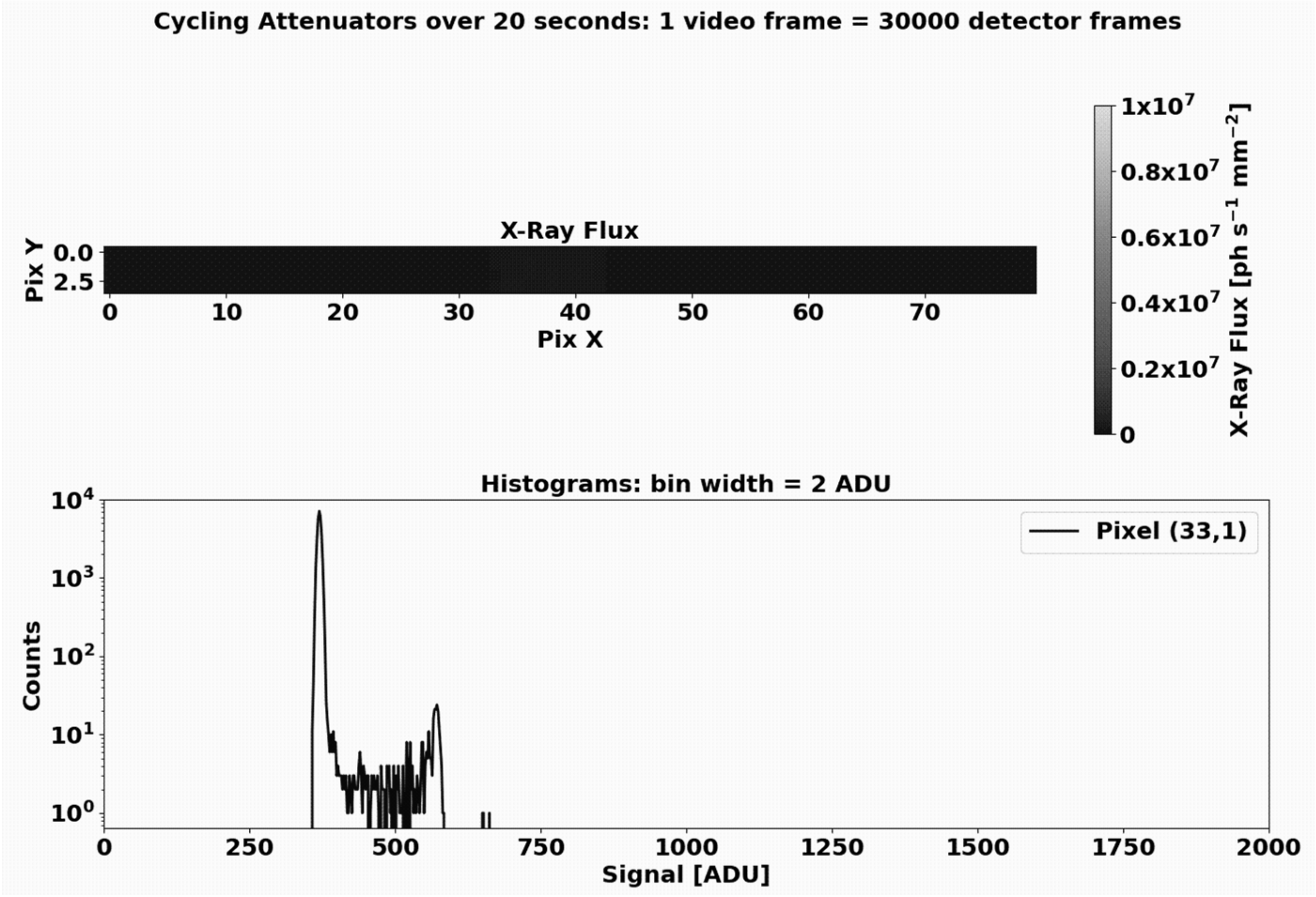
Occupancy across fast-data channel

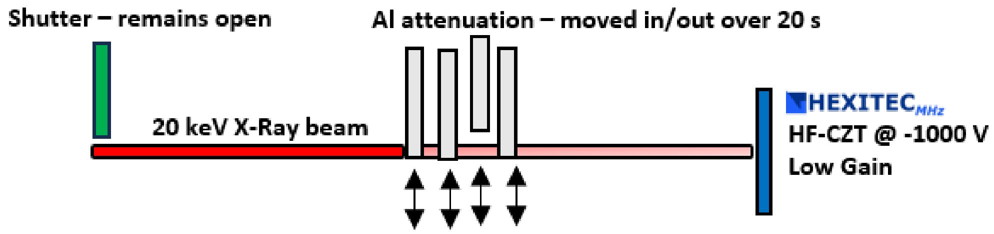


Calibrated histograms of pixel (48,2)

HF-CZT Offset: Dynamic Datasets at diamond

HF-CZT: Changing attenuators over 20 seconds (30 ms/video frame)



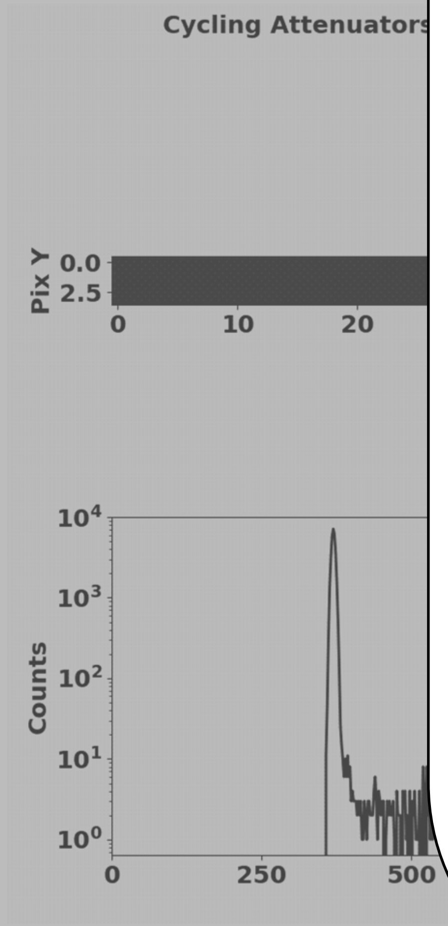


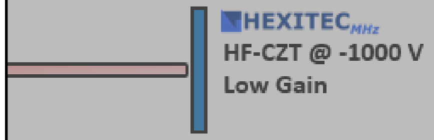
Dynamic measurement schematic

HF-CZT Off... iamond

...oved in/out over 20 s

HF-CZT: Changing at...





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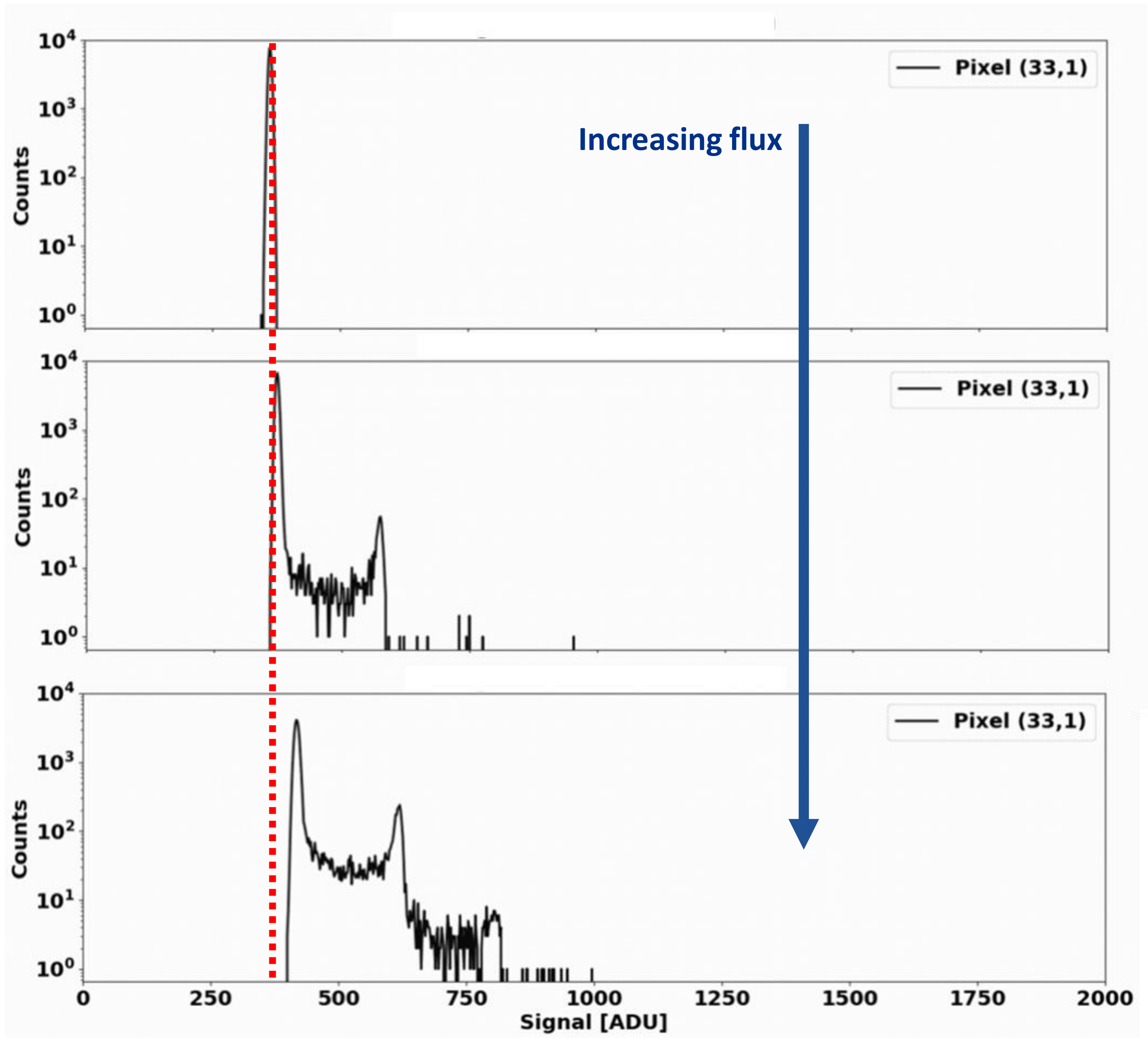
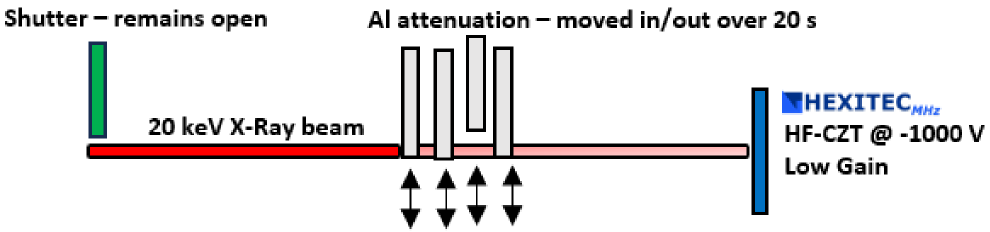
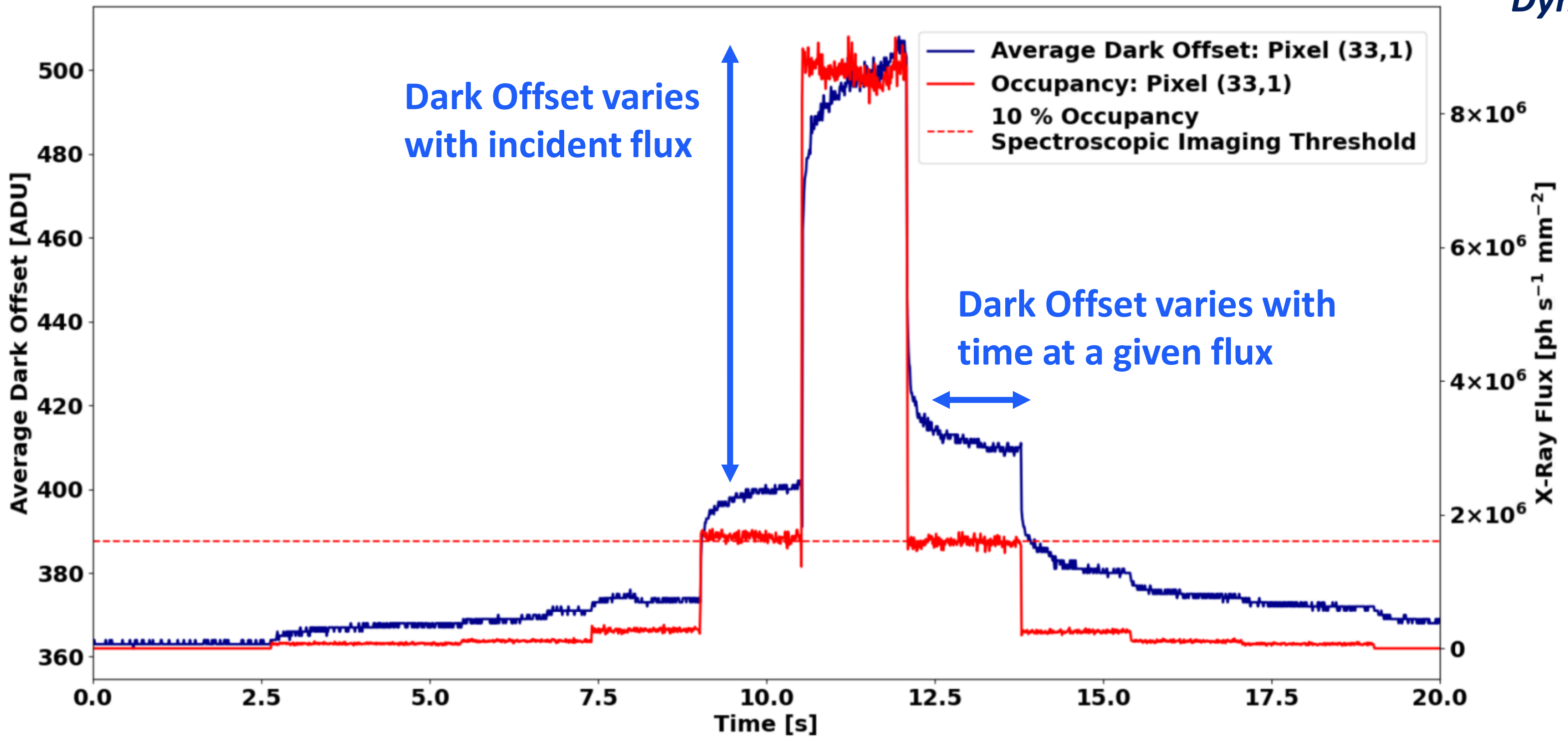


HF-CZT Offset: Dynamic Datasets at diamond

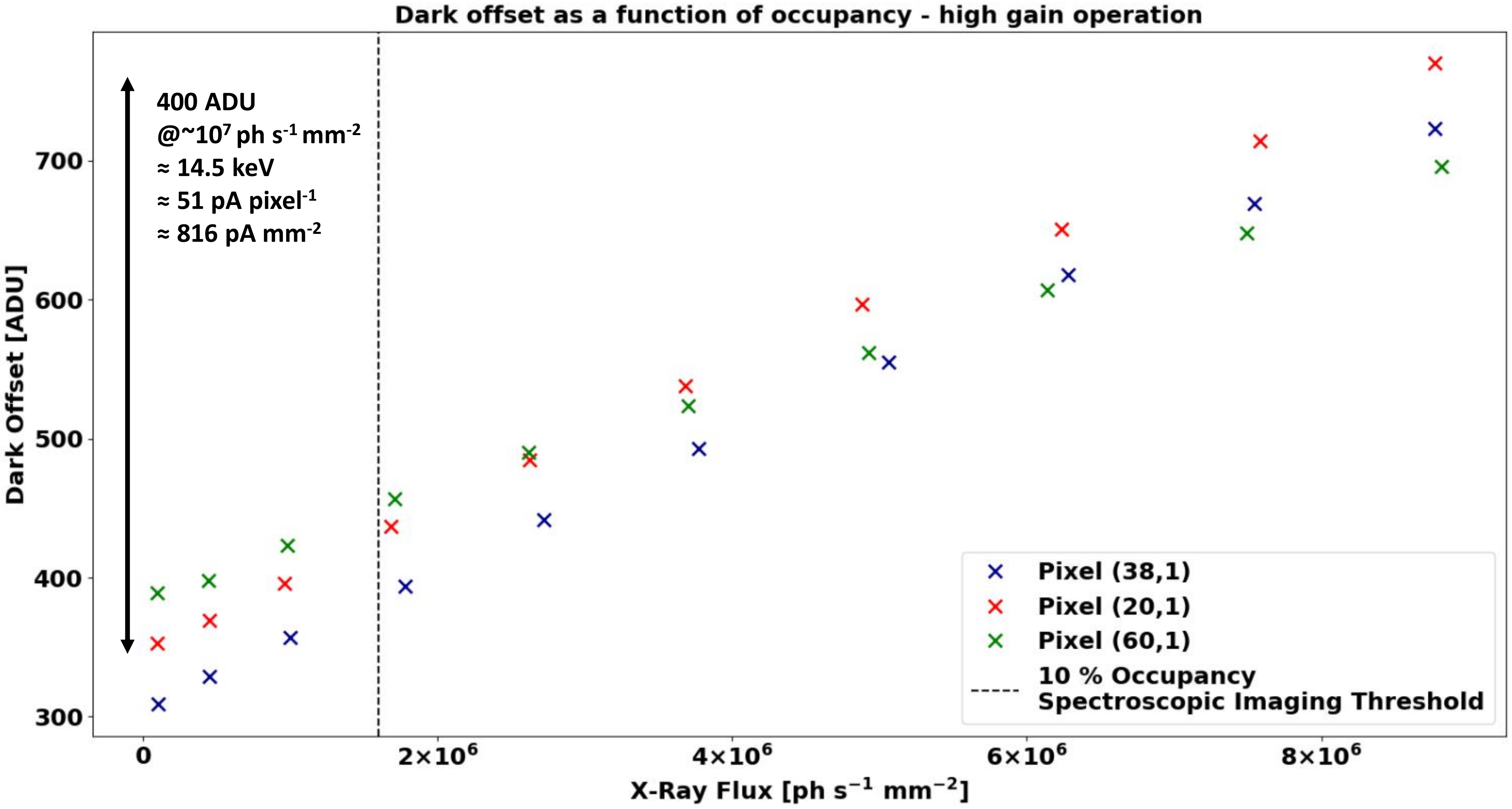


Dynamic measurement schematic

HF-CZT: Changing attenuators over 20 seconds (30 ms/video frame)



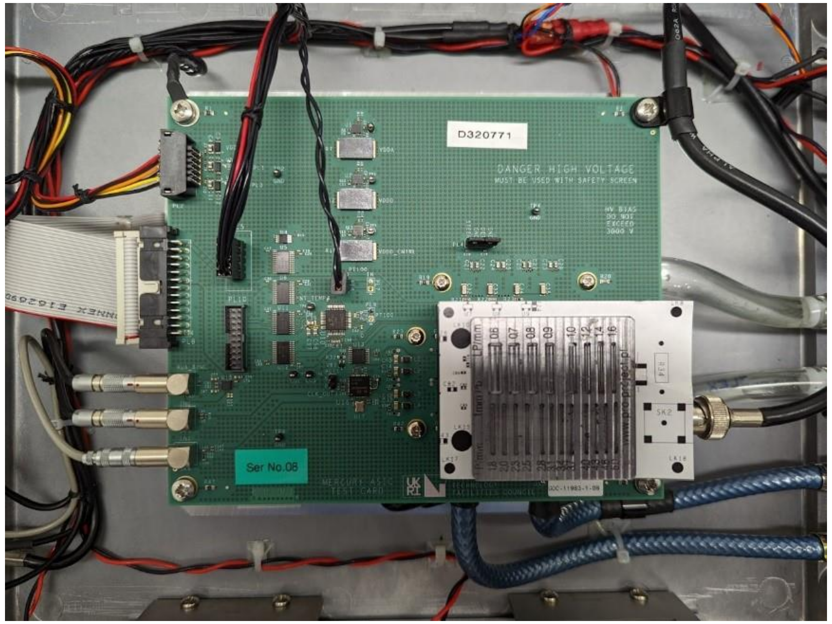
HF-CZT offset: Single-pixel flux scans at diamond



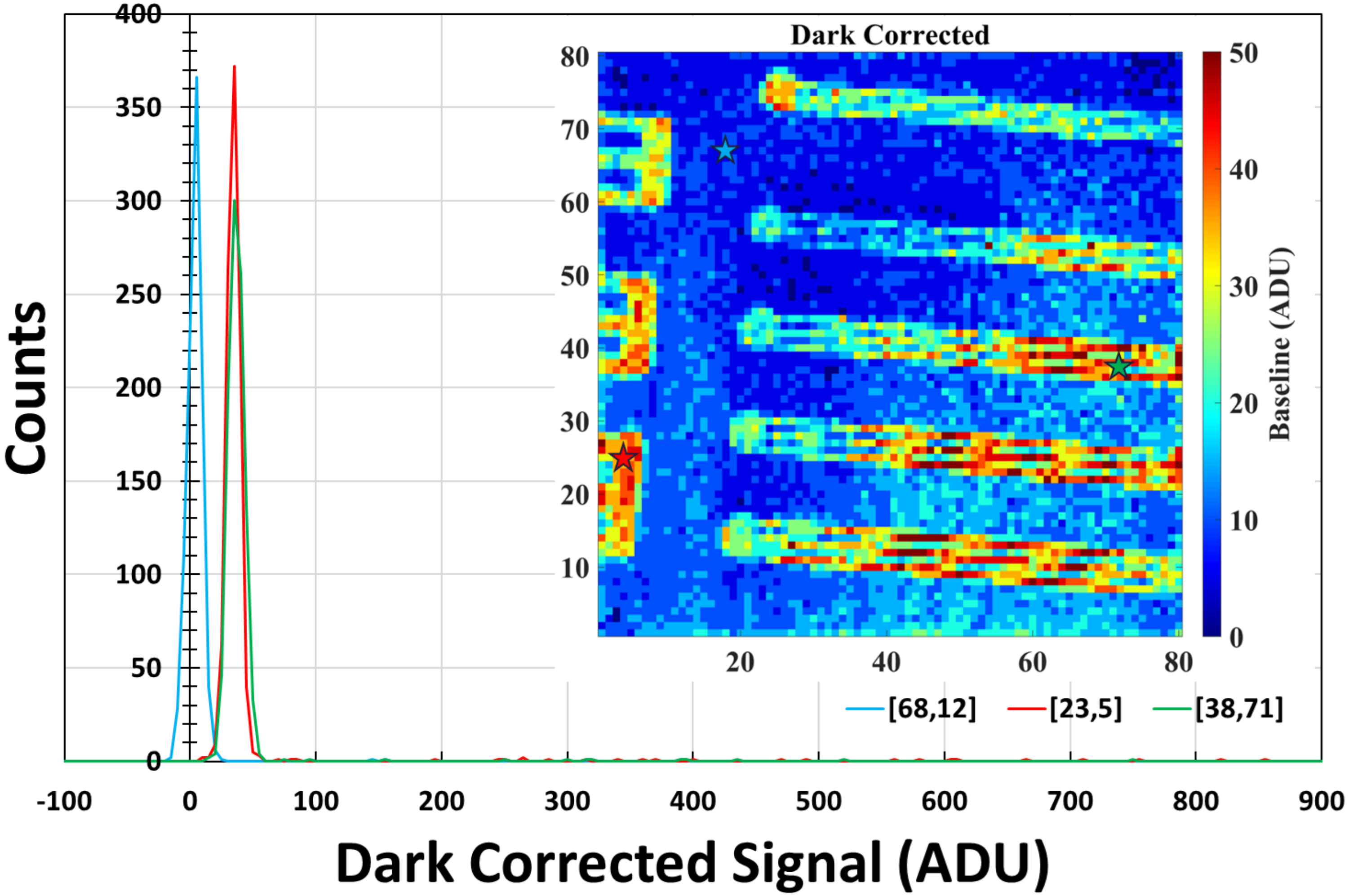
HF-CZT detector @ -1000 V @ 20 keV: Variation of dark offset with X-Ray flux

Real time Xilinx U50 FPGA processing will enable live corrections of this effect

HF-CZT offset: Area scans in laboratory



A lead line pair per mm slide placed over the HF-CZT sensor

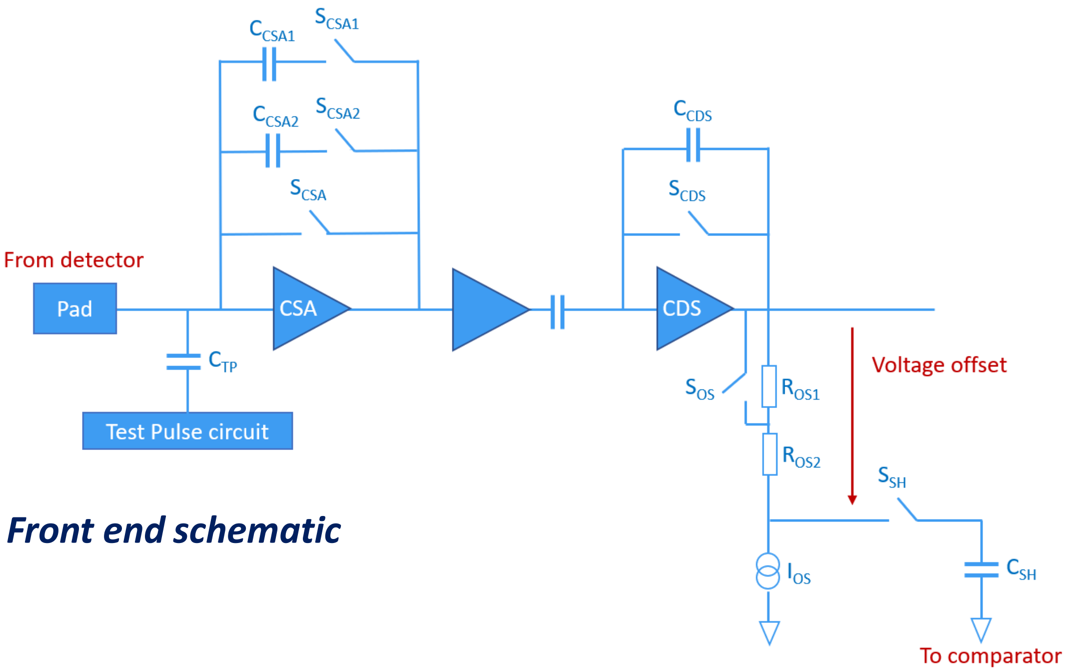


Histograms of signals measured in three pixels from different areas in the irradiation showing different offsets. (Inset) A map of dark-offset

HF-CZT offset: Impeding CSA reset at diamond

1. Impede CSA reset (S_{CSA}) for 10 µs

- ASIC continues outputting every 1 µs



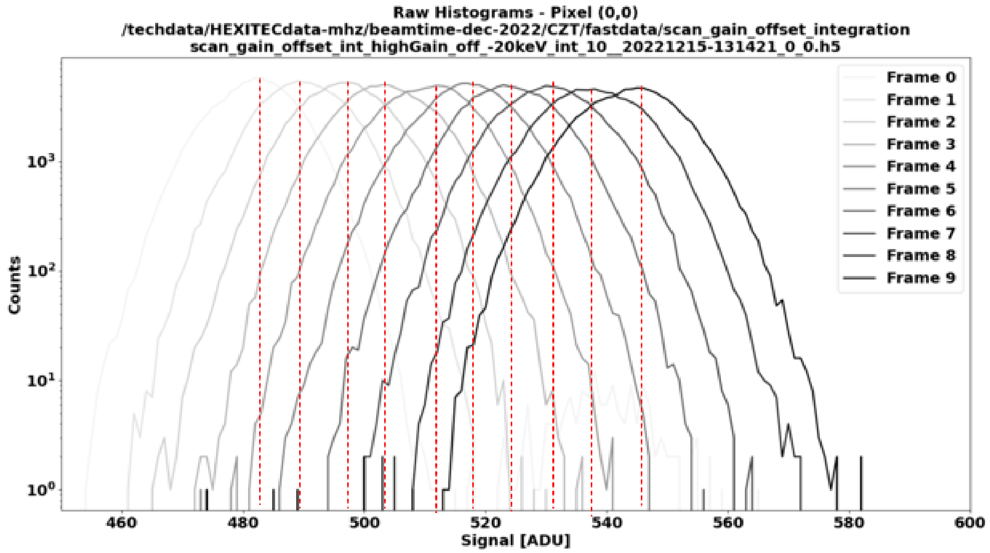
Front end schematic

2. Group and histogram all related frames

- E.g. all 1R frames (1 frame following reset)

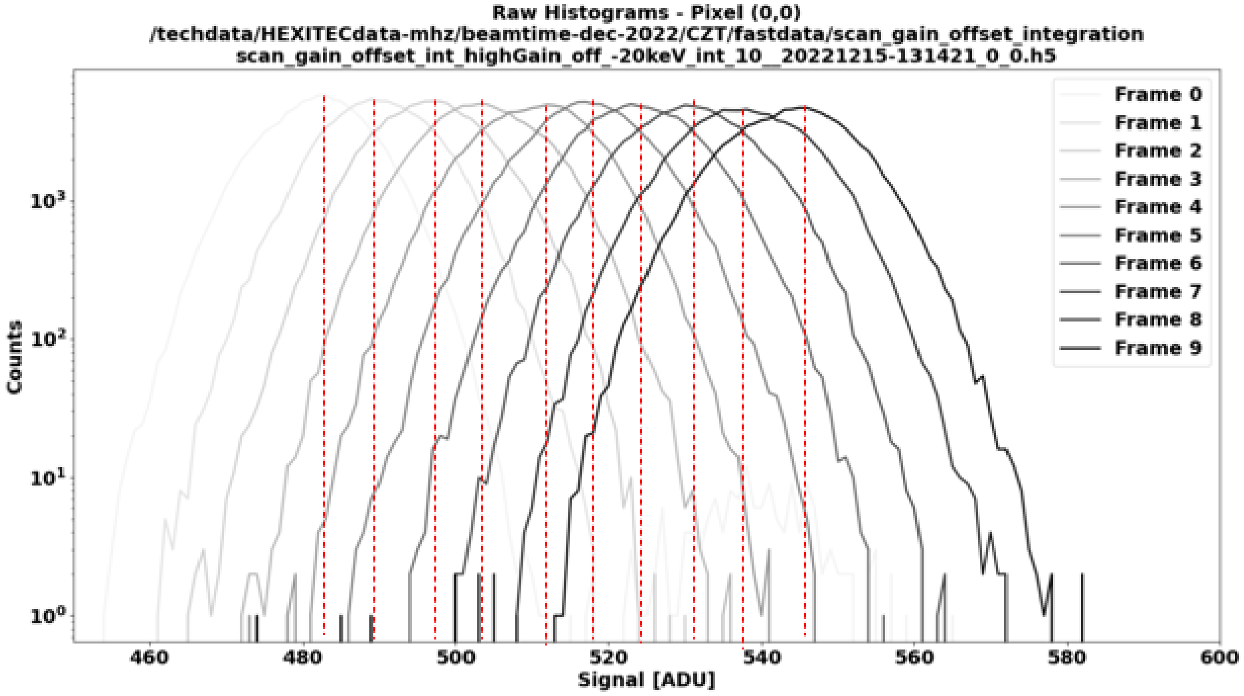
0 *Reset – 0R*	**1** *1R*	**2** *2R*	**3** *3R*	**4** *4R*	**5** *5R*	**6** *6R*	**7** *7R*	**8** *8R*	**9** *9R*
10 *Reset – 0R*	**11** *1R*	**12** *2R*	**13** *3R*	**14** *4R*	**15** *5R*	**16** *6R*	**17** *7R*	**18** *8R*	**19** *9R*
20 *Reset – 0R*	**21** *1R*	**22** *2R*	**23** *3R*	**24** *4R*	**25** *5R*	**26** *6R*	**27** *7R*	**28** *8R*	**29** *9R*

Schematic of frames outputted utilising a 10 µs reset length



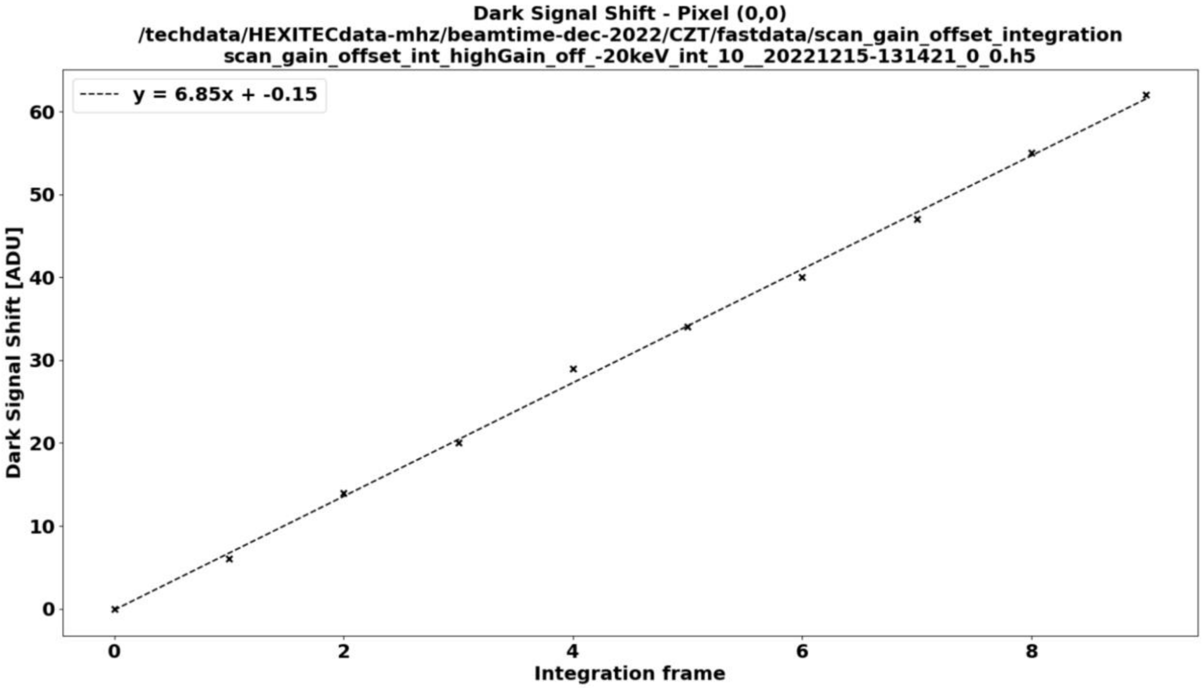
HF-CZT offset: Impeding CSA reset at diamond

3. Identify dark offset for each frame type
- **Shifts to higher ADU as integrating Front-End**



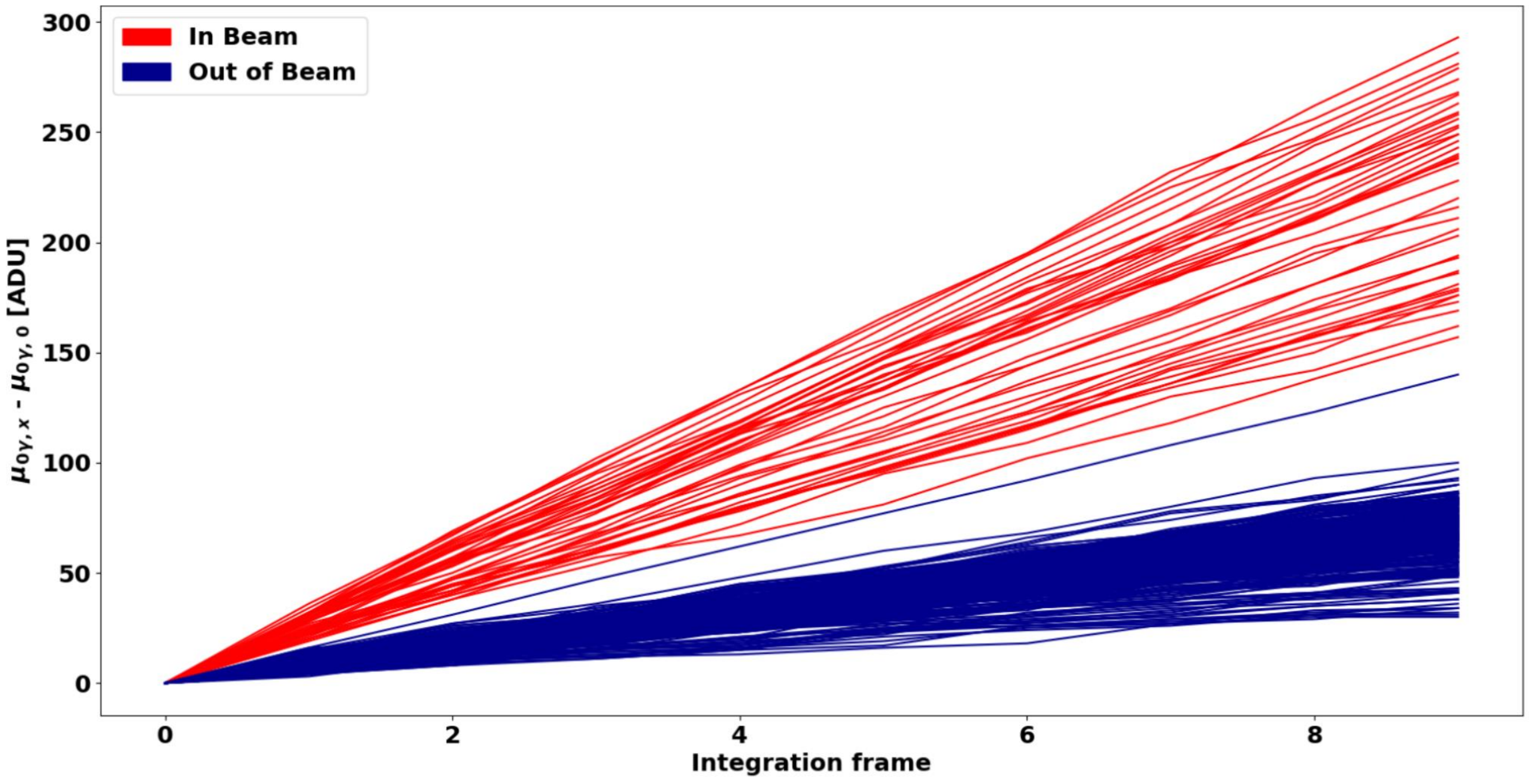
Identification of dark offset for each histogram

4. Calculate linear fit to dark offset vs frames following reset
- **Provides measure of pixel's leakage current**

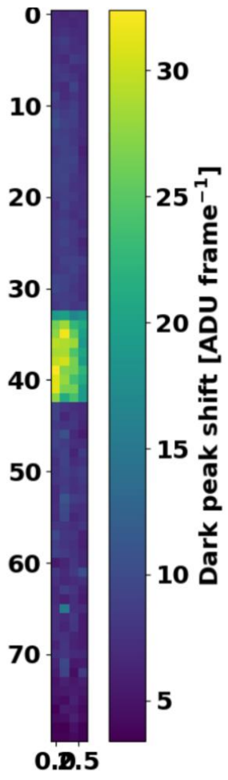


Linear-fit calculation to a plot of dark offset vs frames following reset

HF-CZT offset: Impeding CSA reset at diamond



Corrected dark shift against frames following reset for each pixel in fast-data channel



Map of gradients of calculated linear fits

<u>**Outside of beam – Pixel (0,0)**</u>

Fit gradient - 6.85 ADU frame^{-1}

→ Leakage current = 8.5 pA (136 pA mm^{-2})

- **Typical value for the leakage current**

<u>**Inside of beam – Pixel (40,2)**</u>

Fit gradient – 23.87 ADU frame^{-1}

→ Leakage current = 31.2 pA (500 pA mm^{-2})

- This is a **~24 pA higher than outside of the beam**

Using:
CZT w-factor – 4.6 eV (e-h pair)$^{-1}$
Gradient – 0.036 keV ADU^{-1}
Frame time – 1 μs

Agenda

1 HEXITEC vs HEXITEC$_{MHz}$

The next generation of HEXITEC systems

2 HEXITEC$_{MHz}$ Overview

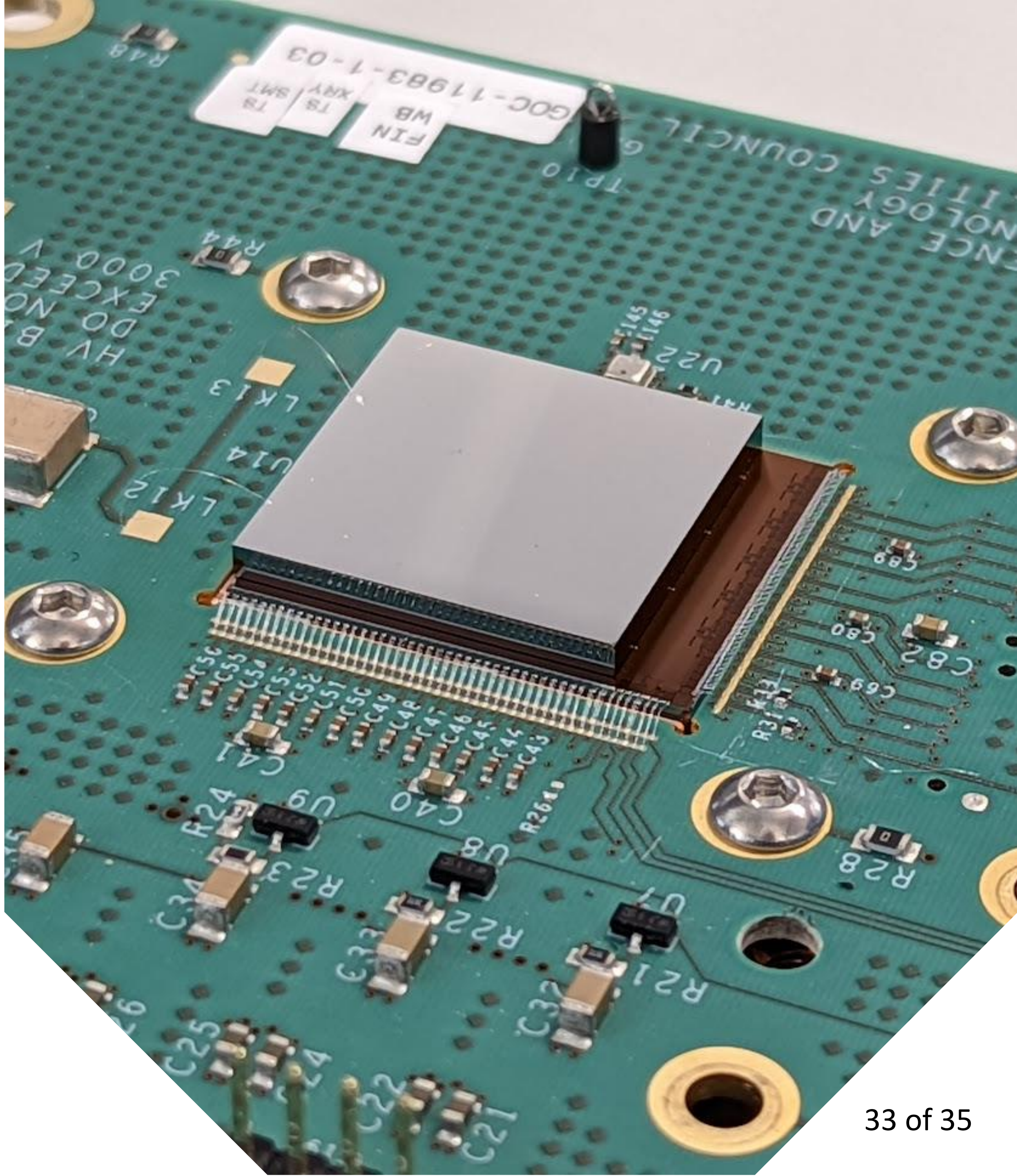
An introduction to our new HEXITEC$_{MHz}$ ASIC including its architecture and specification

3 HF-CZT Test Results

Characterisation of spectroscopic performance using a lab-based X-Ray source and Diamond Light Source synchrotron X-Rays

4 Next Steps

A look to the next 12 months



Next Steps

Achieving a 20-channel fast data output

- Reading out the full 80 × 80 array using the fast data

Further lab-based ASIC and HF-CZT characterisation

- Performance variation across entire active area
- Continued study of observed offset effect

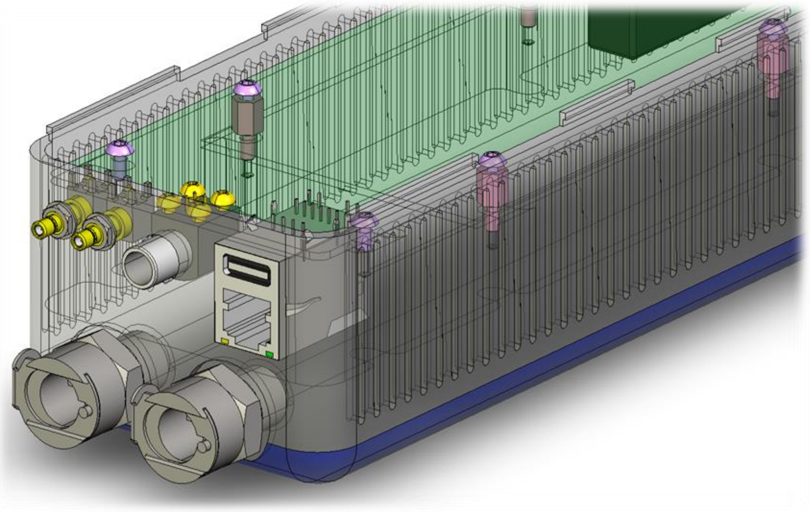
Implementation of in-FPGA histogramming

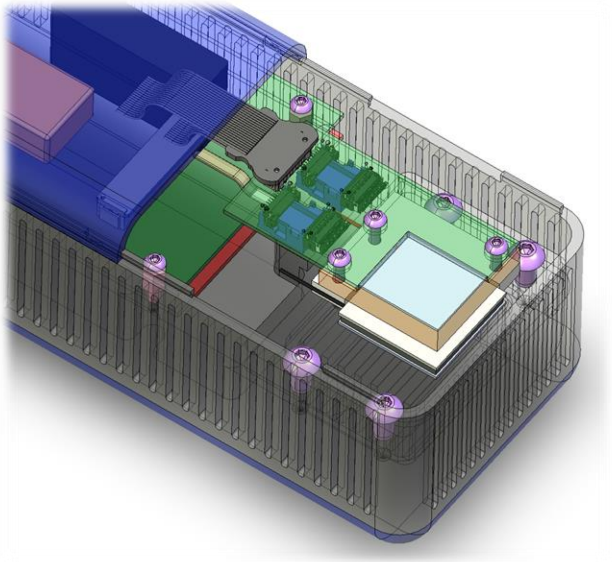
- Orders of magnitude reduction in output data
- Live correction of observed offset effect

Delivery of HEXITEC$_{MHz}$ detector system

- Smaller, form factor production-grade system

Delivering Science





Possible designs for HEXITEC$_{MHz}$ detector system

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Summary

- $HEXITEC_{MHz}$ is a fully-spectroscopic X-Ray detector capable of operating continuously at 1 MHz

Parameter	$HEXITEC_{MHz}$
Max Frame Rate (MHz)	**1**
Max Spectroscopic Flux (ph s^{-1} mm^{-2})	**$>10^6$**
Digitisation	**On-chip**
Detector Type	**Integrating**
Measured FWHM (High Gain)	**0.85 keV @ 20 keV in HF-CZT** **0.68 keV @ 15 keV in p-type Si**

- The next year will include delivery of a full 80 × 80 pixel readout and a new smaller form-factor system

- $HEXITEC_{MHz}$ has been used to observe and investigate a flux-dependent dark offset within Redlen HF-CZT
    - Investigation into this phenomenon is continuing.

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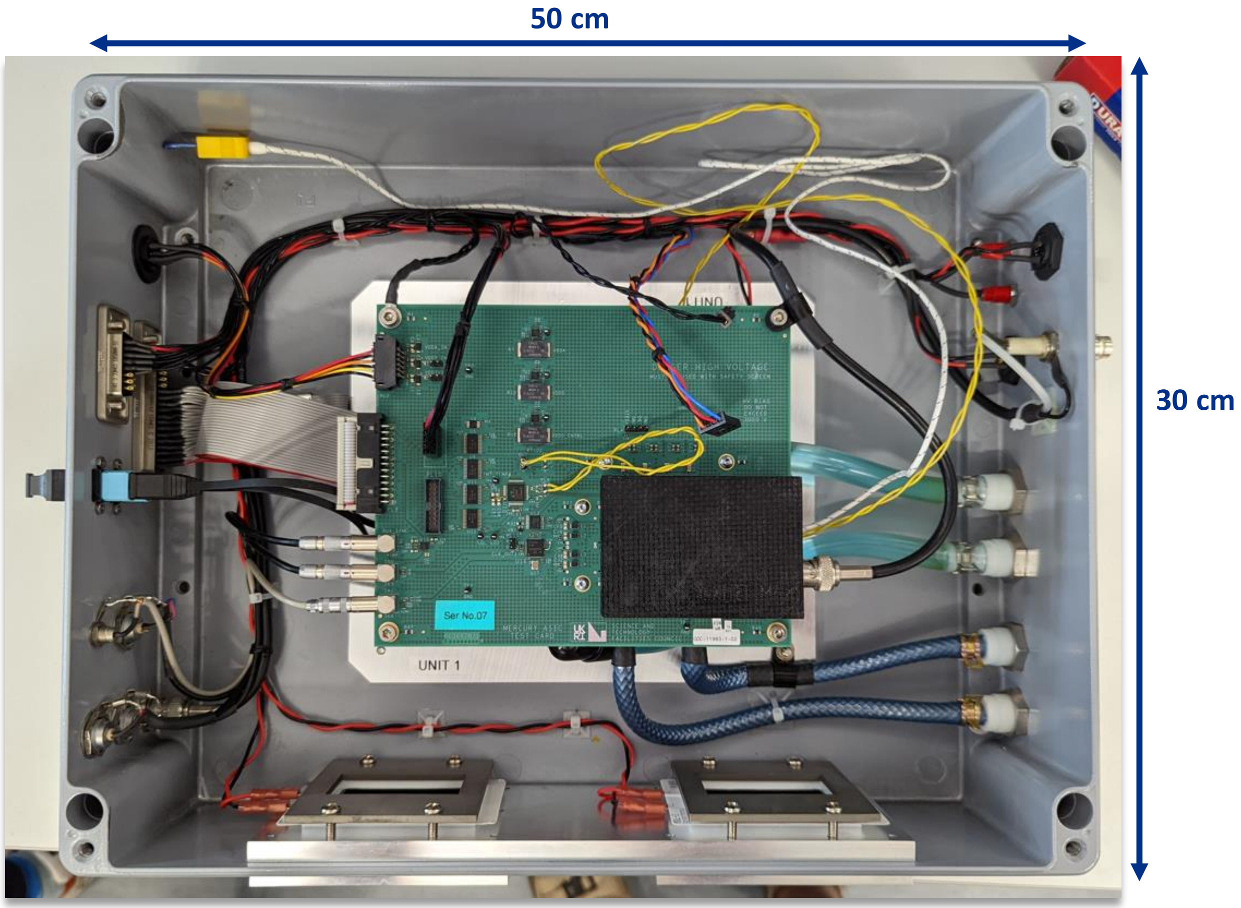
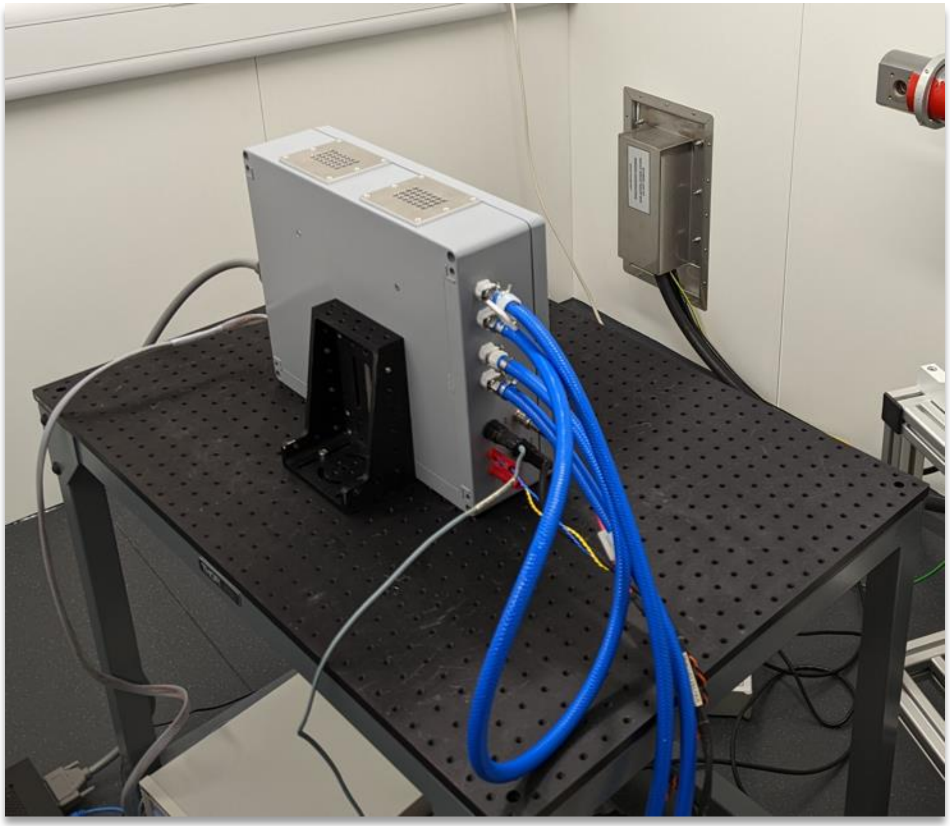
If you have any further questions, please contact me at: ben.cline@stfc.ac.uk

Backup Slides

Testing – Test Setup



HEXITEC$_{MHz}$ test enclosure (interior)



HEXITEC$_{MHz}$ test enclosure (exterior)

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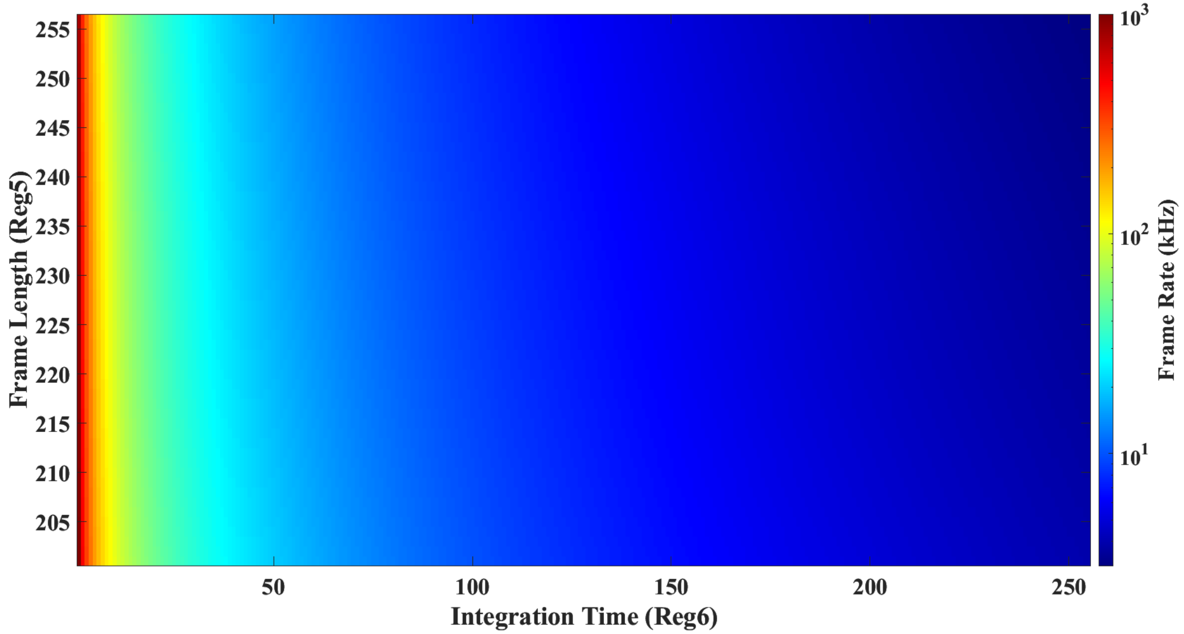
Available Frame Rates

- **Two chip registers can be altered**:
  - Frame Time: **200**→255 clocks frame^{-1}
  - Integration Length: **1** →255 frames

Default values



Available Frame Rates

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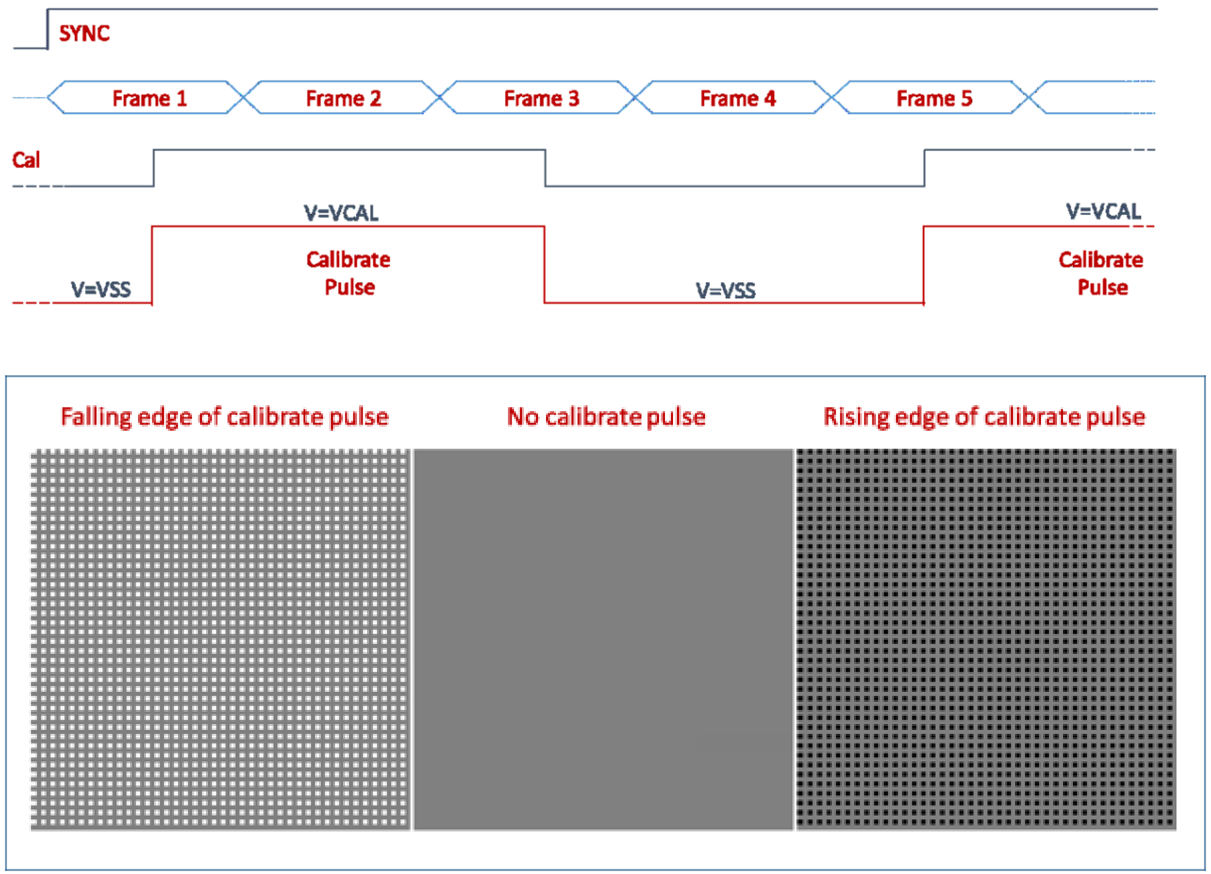
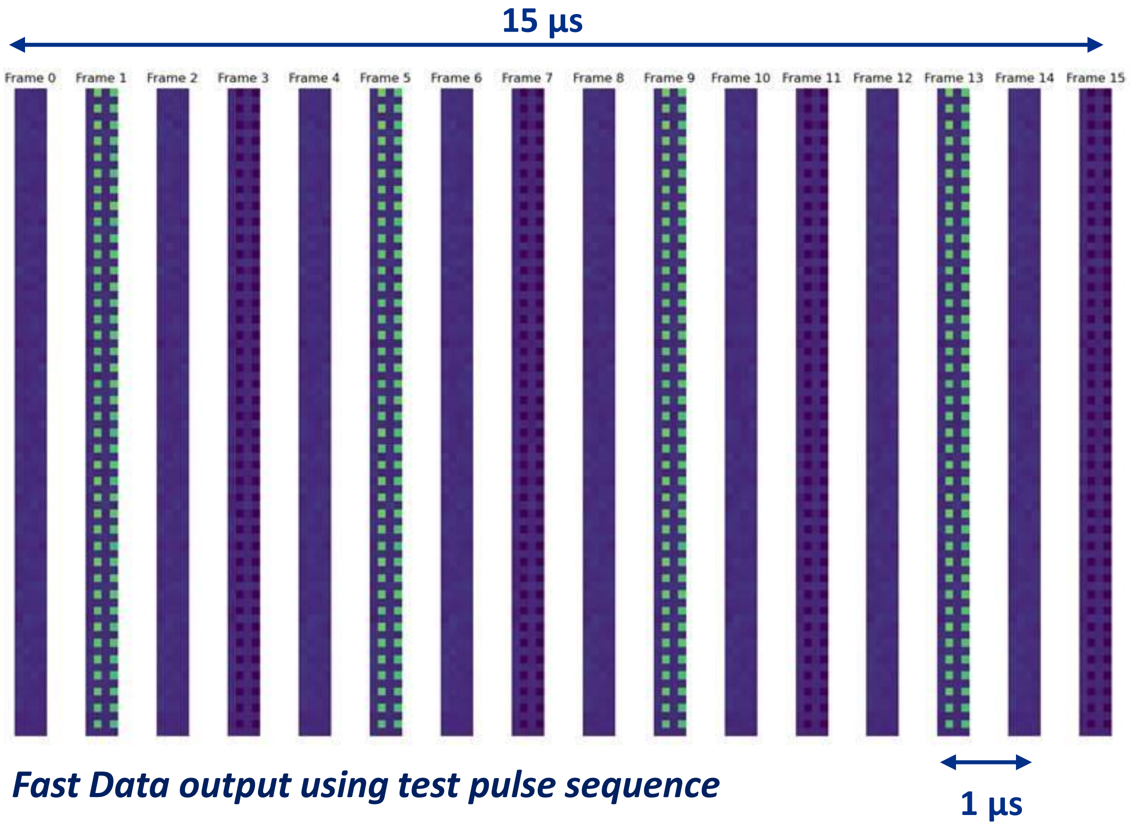
Test Pulse Sequence



Test pulse sequence



Fast Data output using test pulse sequence

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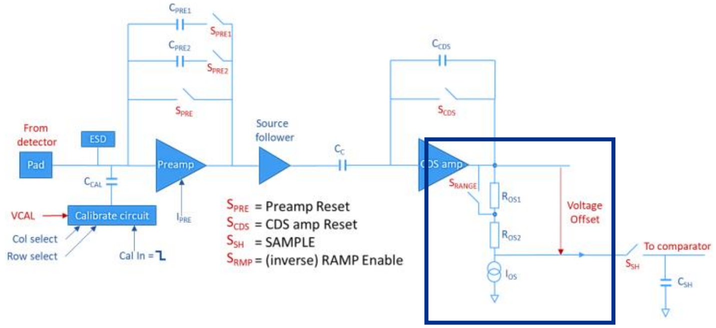
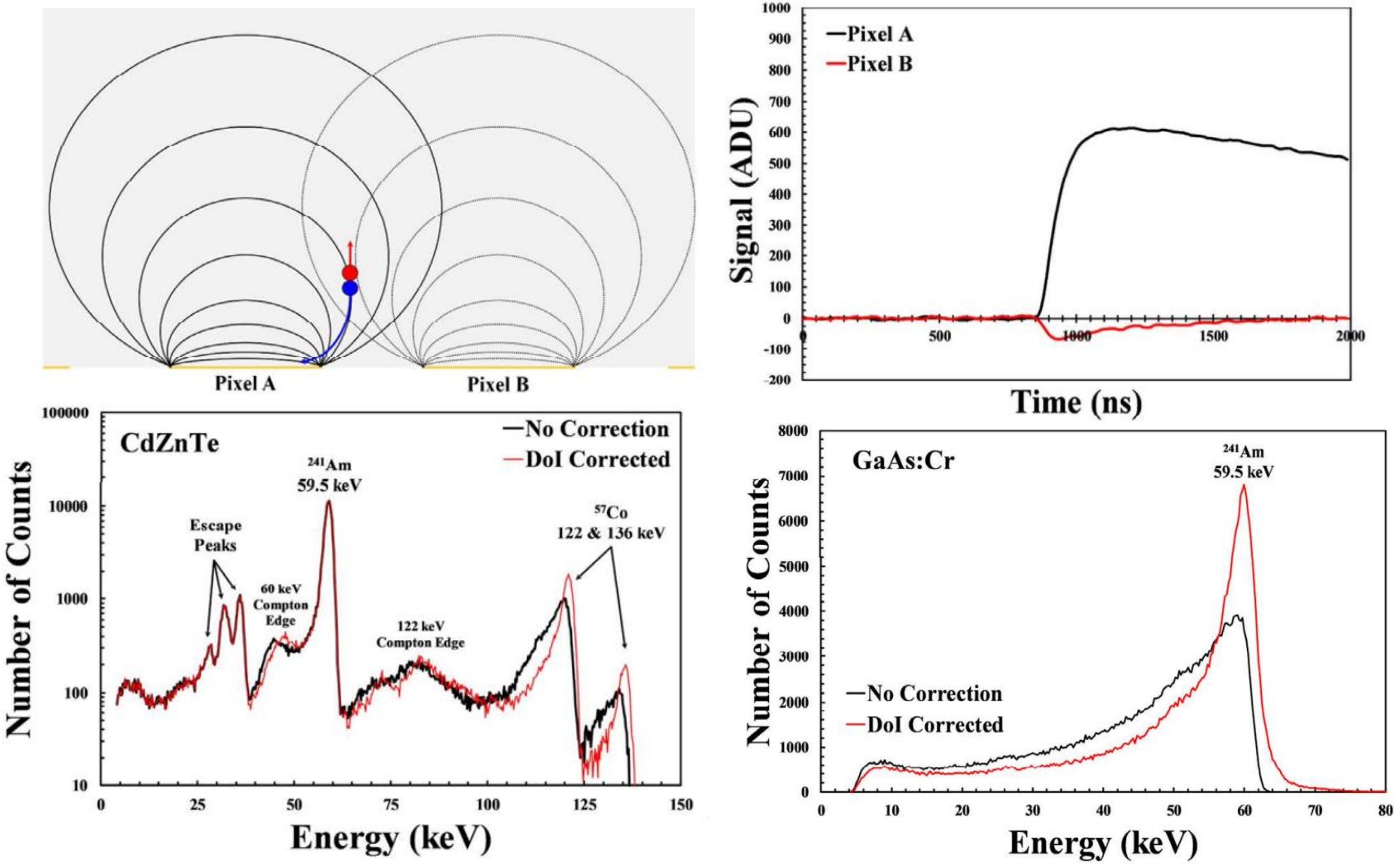
Front End – Negative Offset Circuit



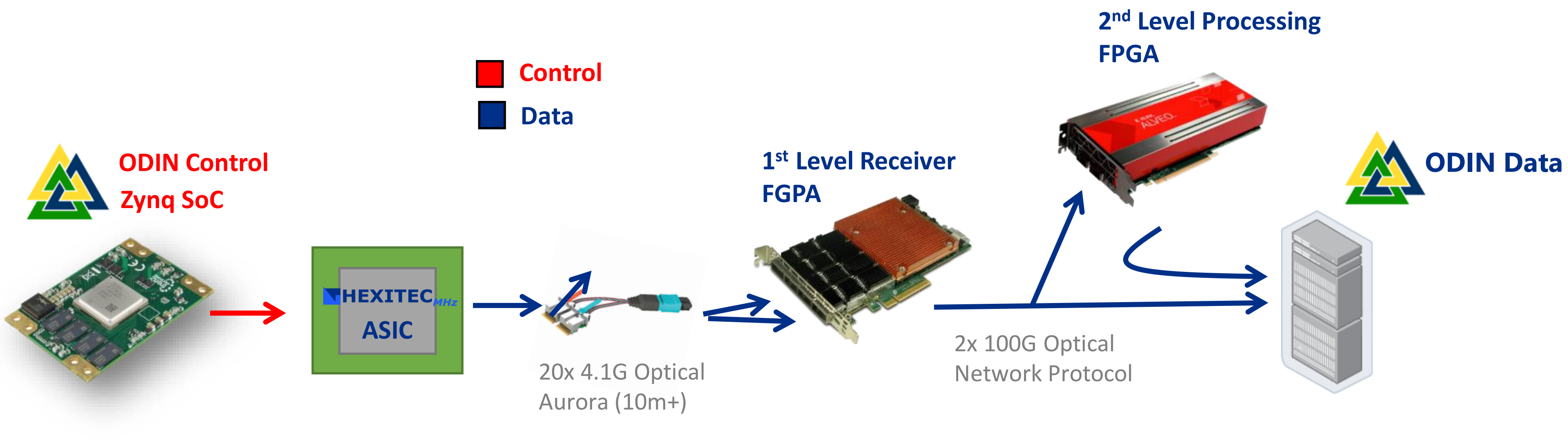
Negative offset circuit

Potential application - Results from Veale et al., 2019;

- **Data collected with STFC's PIXIE ASIC** (DOI: 10.1016/j.nima.2019.01.045)



Data Output Plane



Data output path schematic

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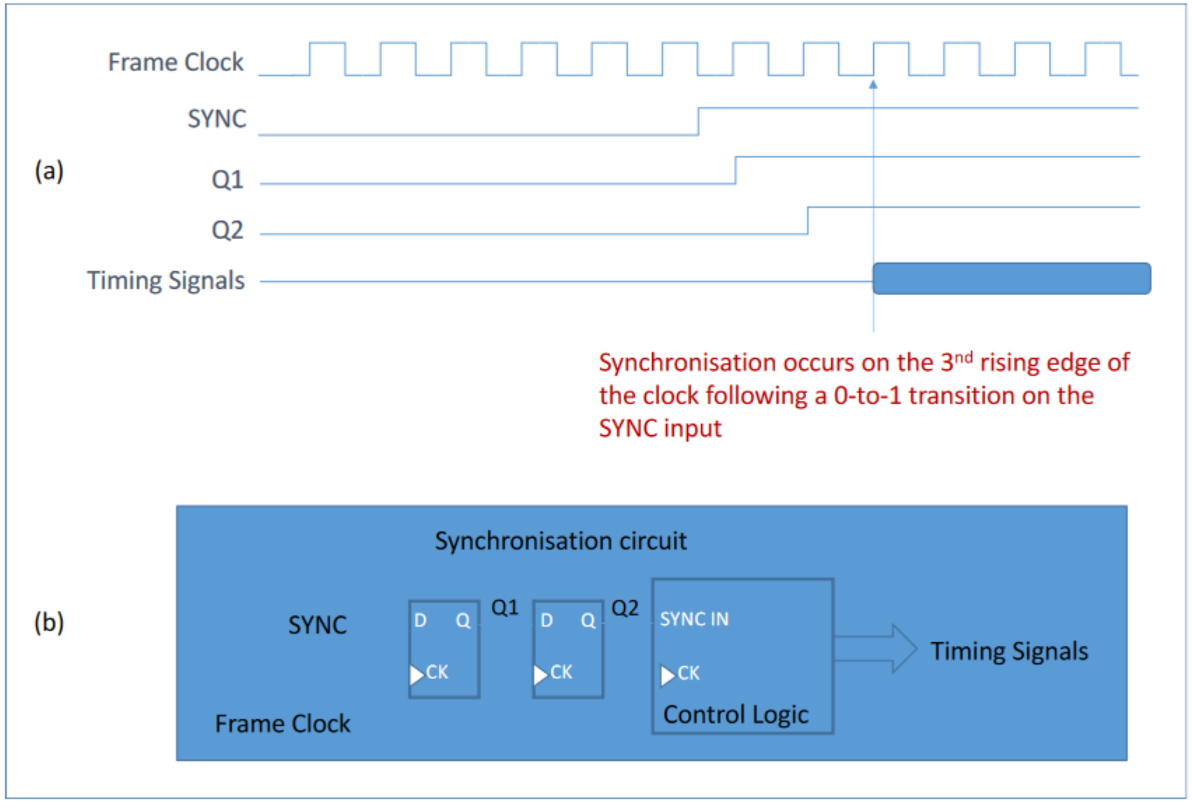
Synchronising the ASIC



Synchronisation circuit

- ASIC synchronised by **controlling transition of SYNC input**
  - Logic 0 → logic 1
  - Synchronisation occurs on 3rd subsequent rising clock edge
- Used for external synchronisation and multi-ASIC systems

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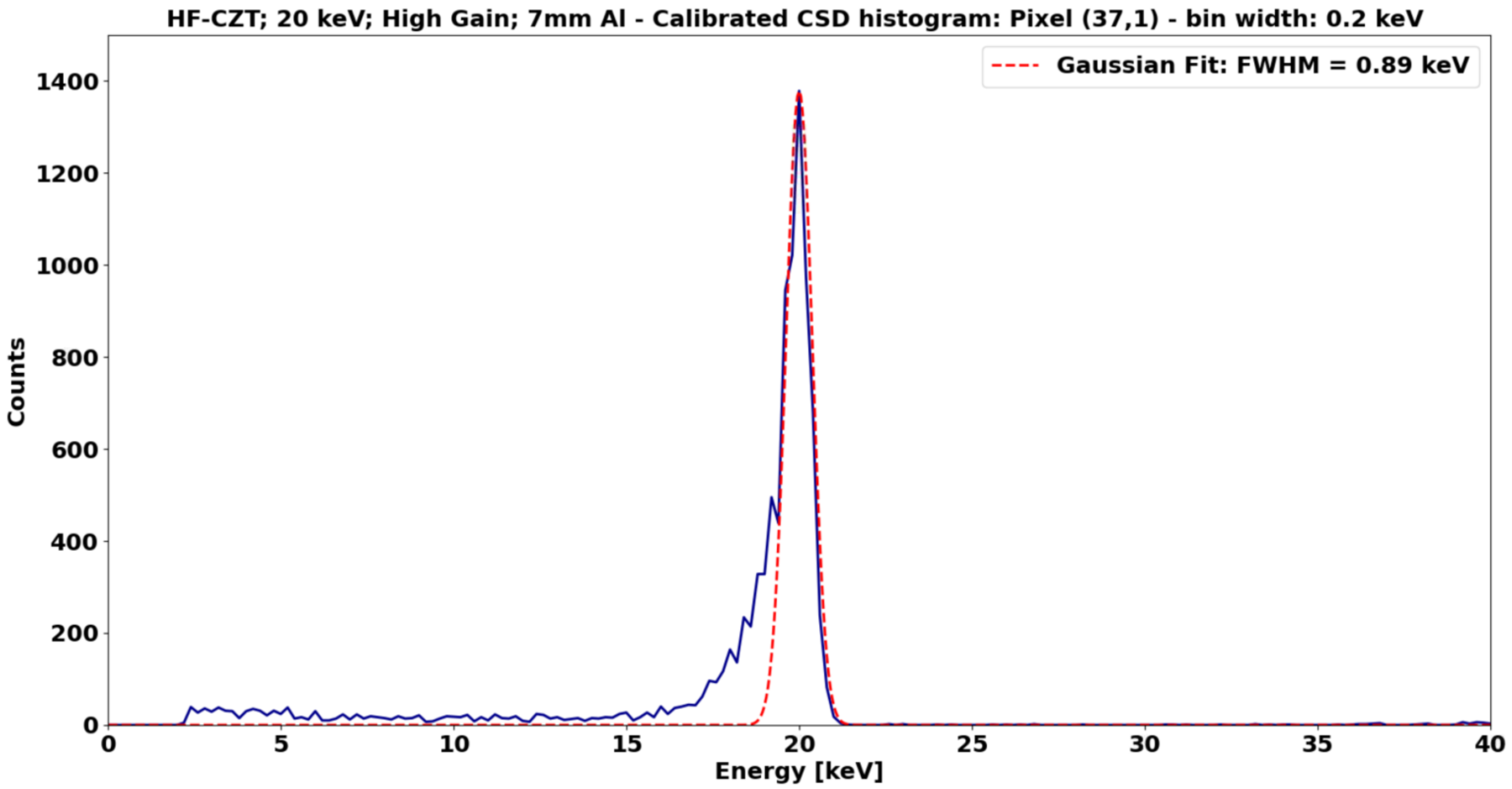
Electronic Noise Contribution



- HF-CZT FWHM @ 20 keV ≈ 0.9 keV
- HF-CZT w factor = 4.67 eV
- → ENC = $\sqrt{900 \times 4.67} \approx 65\ e^-$

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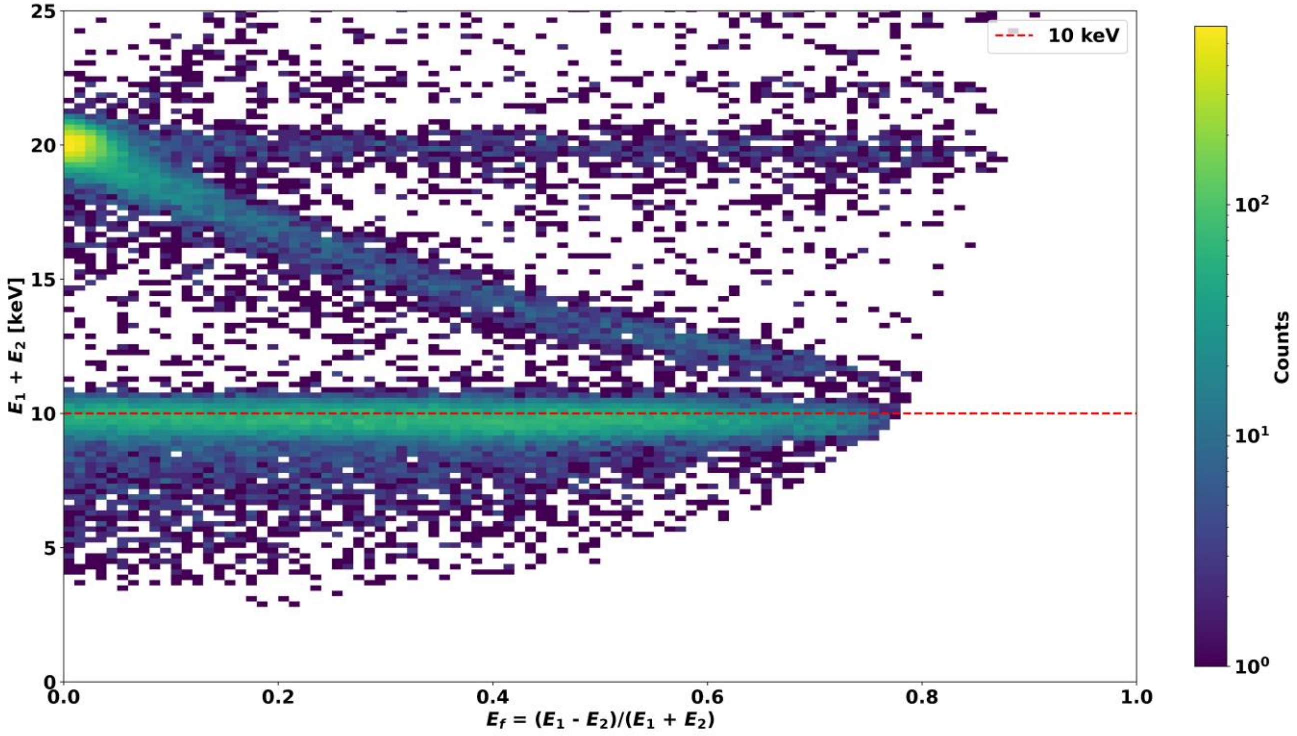
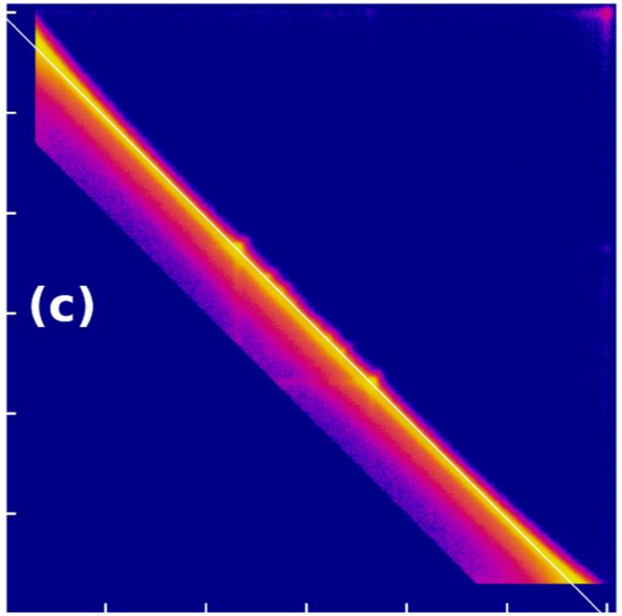
diamond – Charge Sharing

P-type Si; 10 keV; High Gain; ~2 % occupancy; 0.2 keV bin width



The distribution of energies in two-pixel charge sharing events using a 10 keV beam energy at an occupancy of ~2% - 0.2 keV bin width

HF – CdZnTe
Frame occupancy : 0.4%



Open Access | Article

Charge Sharing and Charge Loss in High-Flux Capable Pixelated CdZnTe Detectors

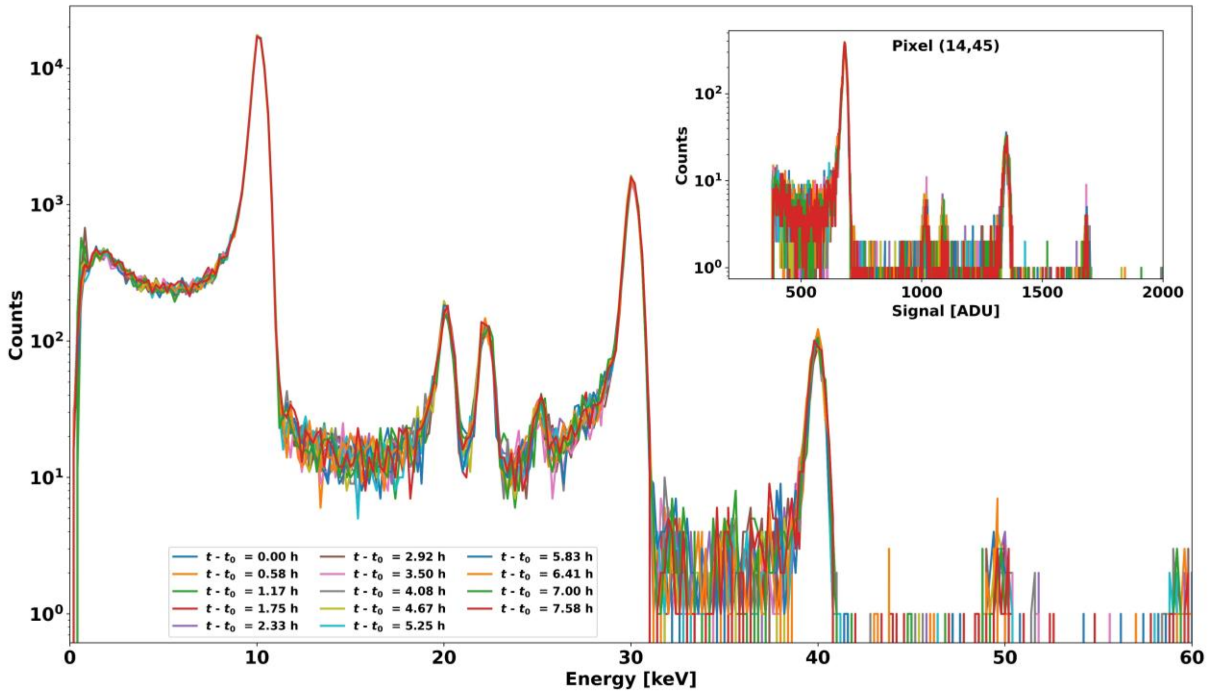
by Kjell A. L. Koch-Mehrin [1,*], Sarah L. Bugby [2], John E. Lees [1], Matthew C. Veale [3] and Matthew D. Wilson [3]

1 Space Research Centre, Department of Physics & Astronomy, University of Leicester, Leicester LE1 7RH, UK
2 Centre for Imaging Science, Department of Physics, Loughborough University, Loughborough LE11 3TU, UK
3 STFC Rutherford Appleton Laboratory, Harwell Campus, Didcot OX11 0QX, UK
* Author to whom correspondence should be addressed.

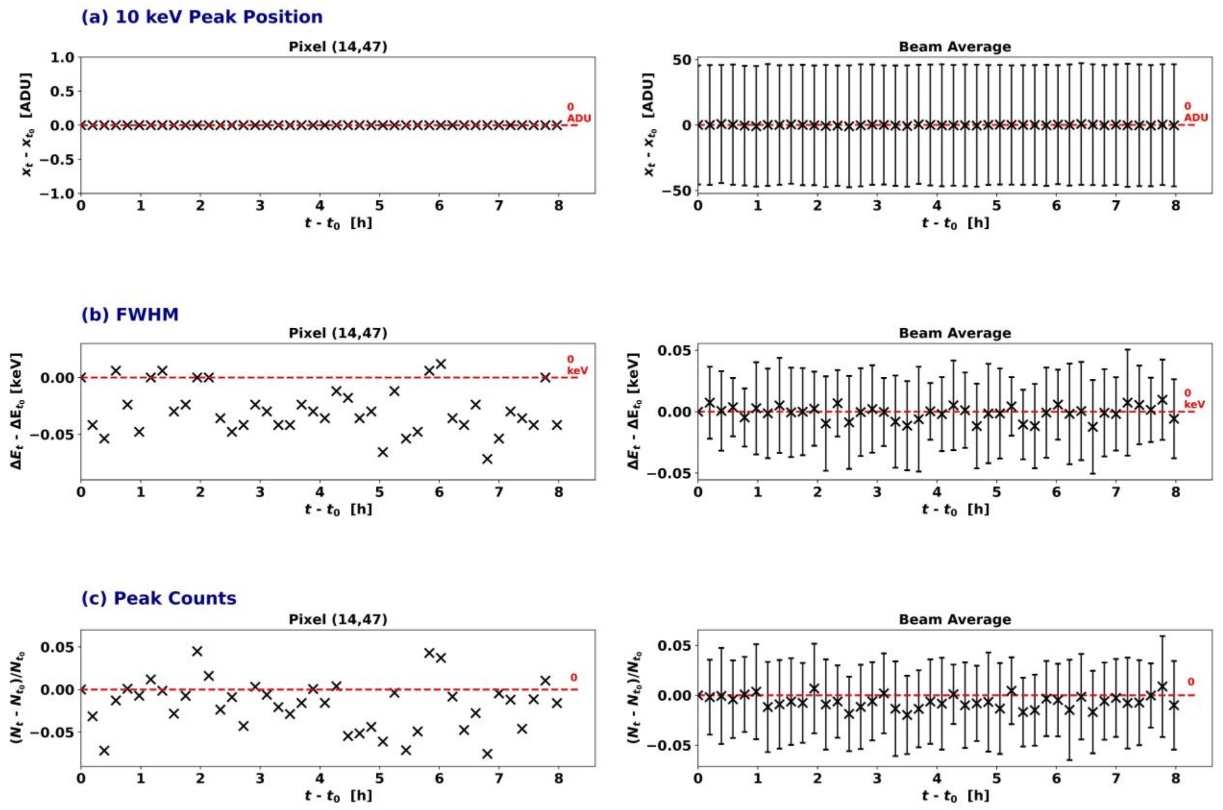
Sensors **2021**, *21*(9), 3260; https://doi.org/10.3390/s21093260

Received: 31 March 2021 / Revised: 26 April 2021 / Accepted: 6 May 2021 / Published: 8 May 2021

diamond – Temporal Stability

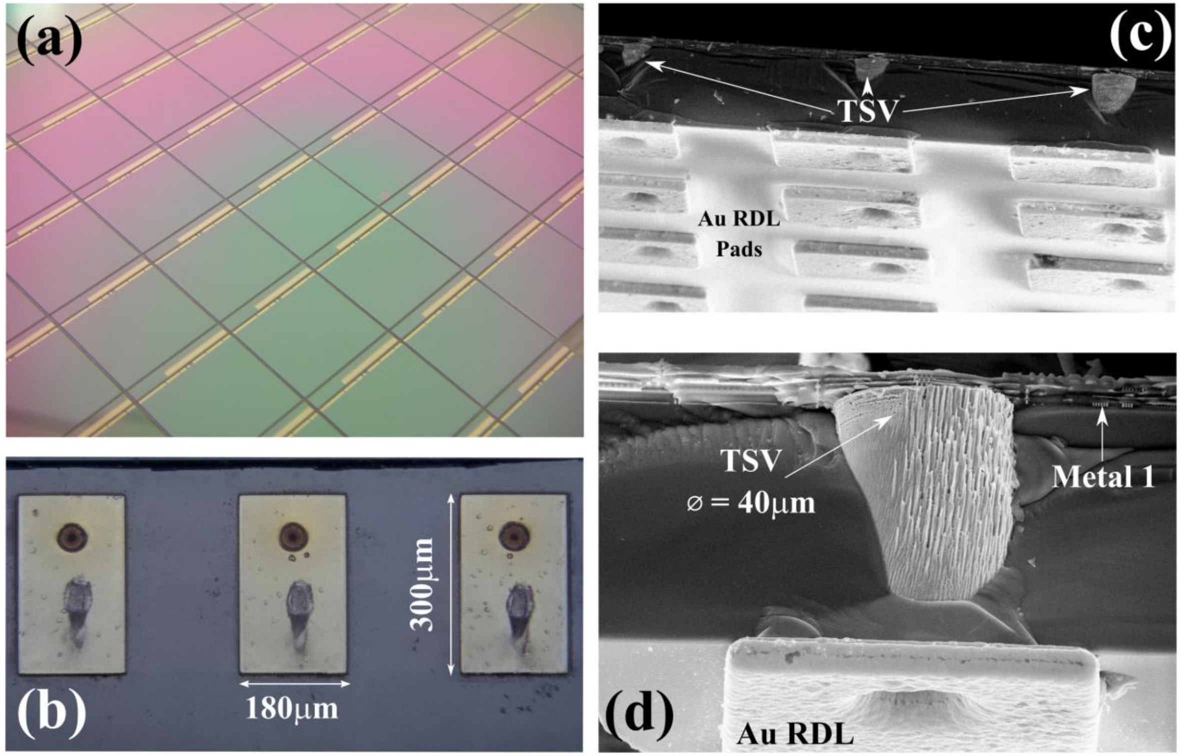


Evolution of high-gain calibrated global CSD spectra during exposure @ 10 keV for ~8 h – 0.2 keV bin width. Inset plot shows uncalibrated CSD spectra for pixel (14,45) – 1 ADU bin width



Change in performance of p-type HEXITEC$_{MHz}$ device during exposure @ 10 keV for ~8 h. Plots show fluctuation in peak position (a), change in FWHM (b), and fractional change in peak counts (c) of 10 keV photo peak. Peak counts comprise events within the FWHM of peak, and error bars given by standard deviation across beam region

TSVs on HEXITEC



(a) I/O pads on reverse of the 200 mm HEXITEC4S wafer post-TSV-last processing. (b) RDL pads dimensions on ASIC's reverse. (c) SEM micrograph of exposed TSVs in cleaved test chip. (d) SEM micrograph showing contact between TSV and ASIC's bottom metal layer

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https://doi.org/10.1016/j.nima.2021.166083

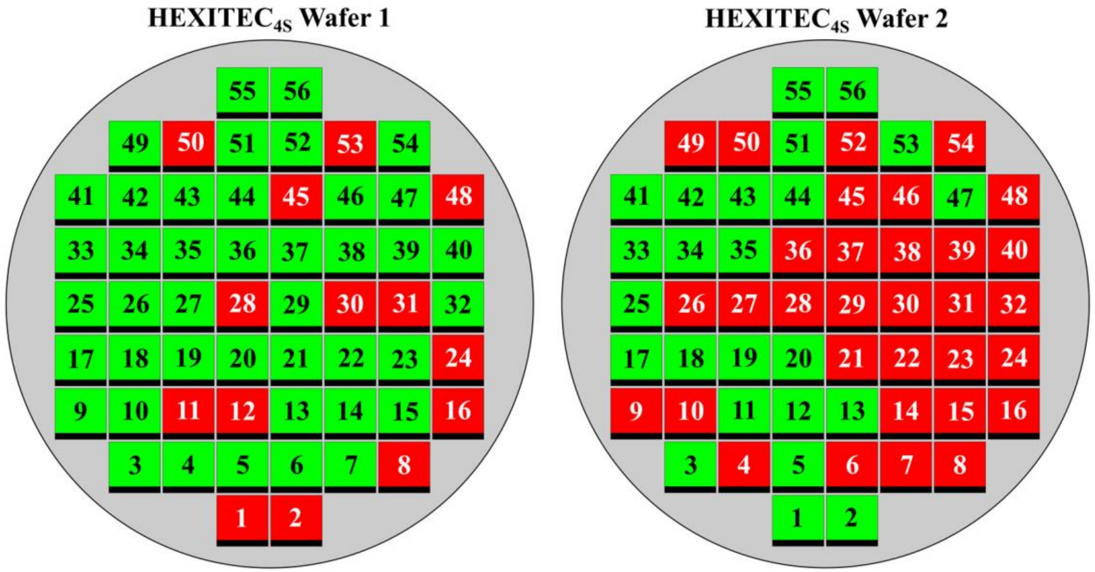
ELSEVIER

Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment

Volume 1025, 11 February 2022, 166083

Characterisation of the HEXITEC$_{4S}$ X-ray spectroscopic imaging detector incorporating through-silicon via (TSV) technology

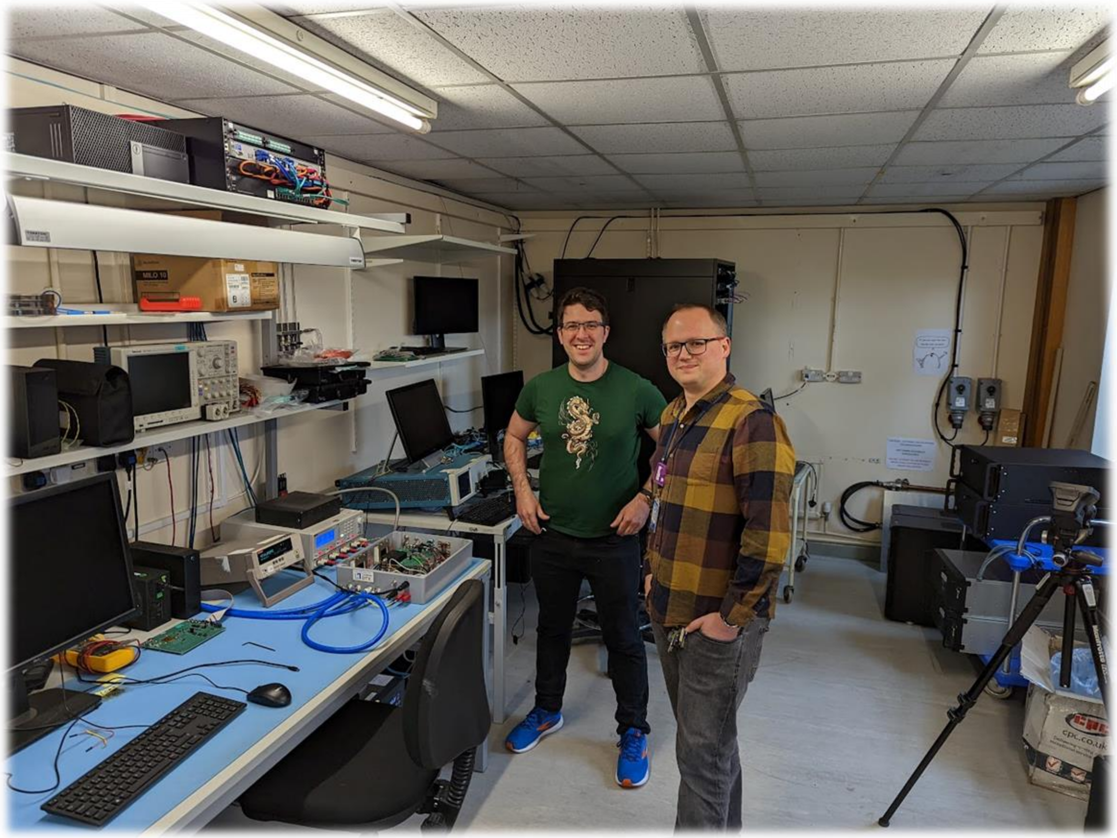
M.C. Veale [a], P. Booker [a], I. Church [a], L.L. Jones [a], J. Lipp [a], A. Schneider [a], P. Seller [a], M.D. Wilson [a], I. Chsherbakov [b], I. Kolesnikova [b], A. Lozinskaya [b], V. Novikov [b], O. Tolbanov [b], A. Tyazhev [b], A. Zarubin [b]



Wafer maps showing results of probe testing. Green – functioning; Red – non-functioning

Next steps – Current Applications

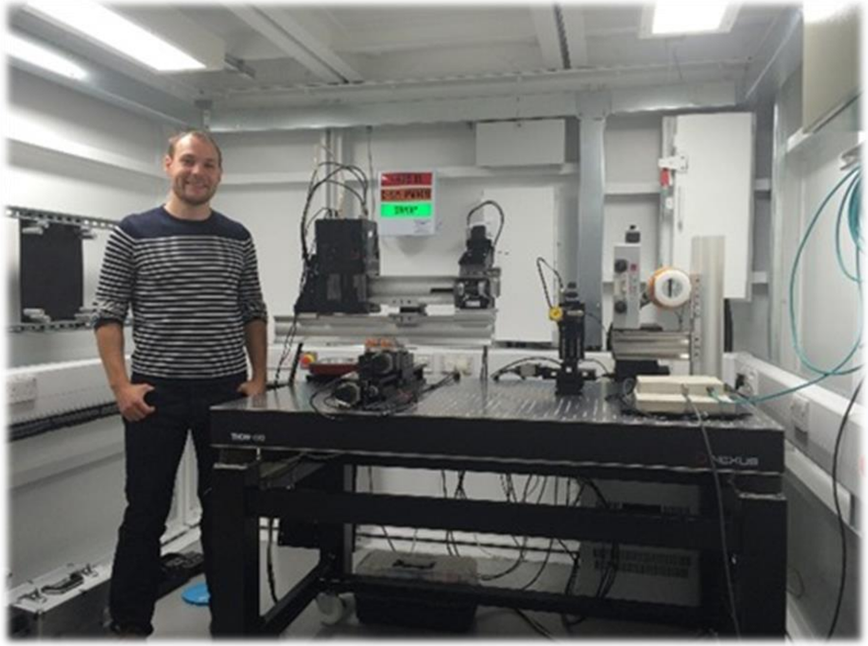
MIC-12-434: *On the feasibility of using HEXITEC$_{MHZ}$ and fully-spectral x-ray imaging to detect breast tumours: an in-silico study*



The ROYAL MARSDEN
NHS Foundation Trust

ICR The Institute of Cancer Research

New Project: 5DCT – *Dynamic Colour X-ray Computed Tomography*

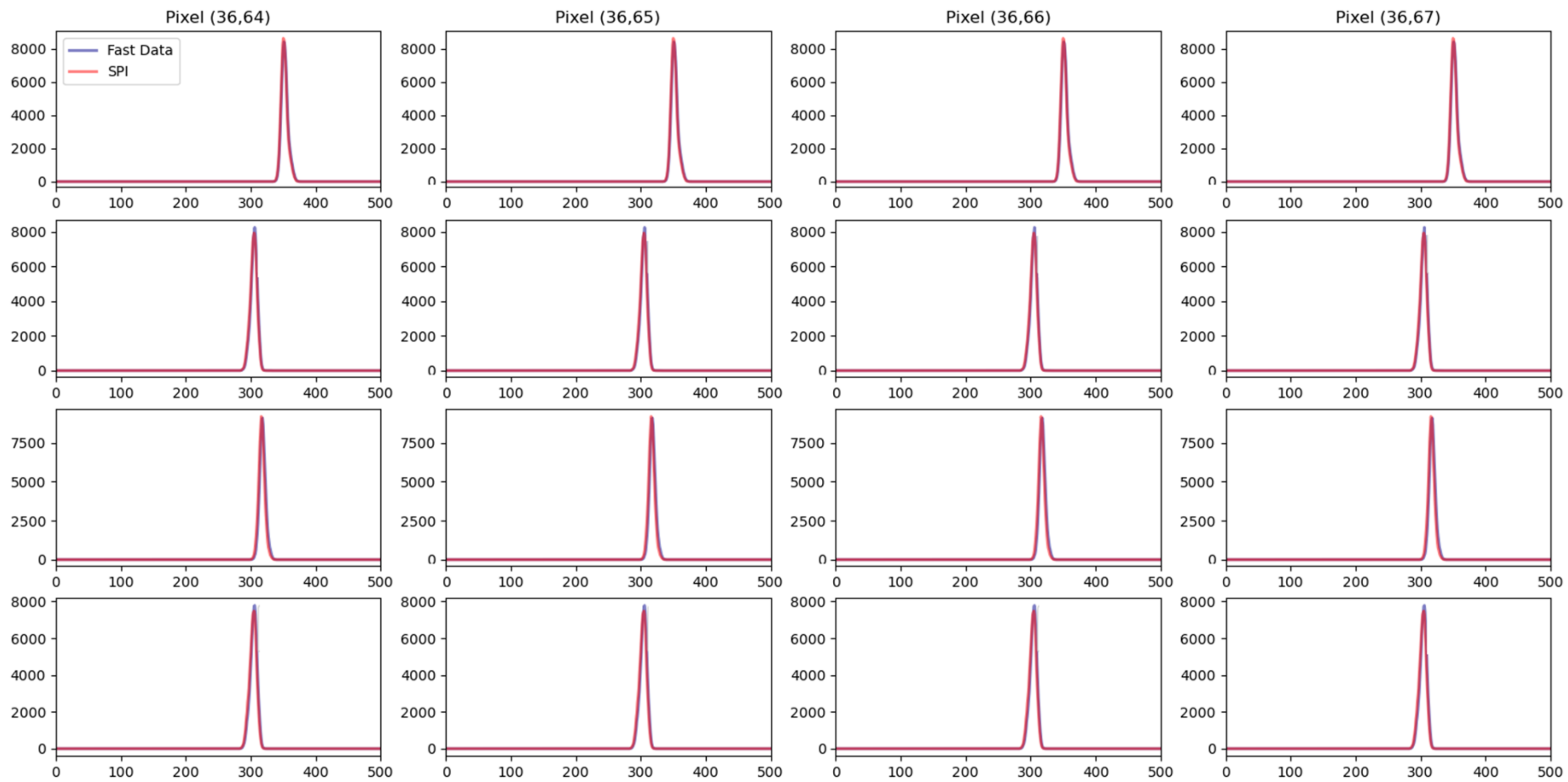


NXCT National X-Ray Computed Tomography

Department for Business, Energy & Industrial Strategy

UKRI Biotechnology and Biological Sciences Research Council

Testing – SPI vs Fast Data Comparison



Comparison of fast data and SPI measurements using test pulse

Fast data matches SPI output ☺

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